ARCHIVO DE PRUEBAS
OMICRON

AUDITORIA TECNICA DE EQUIPOS DE PROTECCIONES.

PROTECCION DE FALLA INTERRUPTOR - UNIDAD DE CAMPO 01 (52J2) EN S/E NUEVA MAITENSILLO
MODELO 7SS523, MARCA SIEMENS

INGEMA S. A		**CLIENTE**	
Probado por: Ing. Mario Aguilar	Revisado por: Ing. Antony Porras	Recibido por:	Aprobado por:
Fecha: 09-04-2019		Fecha:	Fecha:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J2	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Hadware

Test Equipment

Type	Serial Number
CMC356	??????

Hardware Check

Performed At	Result	Details
Not yet performed		

Group:1. Verificacion Medida Fase L1

2.1 Inyeccion 25% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time: 20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:48:33	Test End:	11-abr.-2019 02:50:04
User Name:		Manager:	
Company:			

Test Results

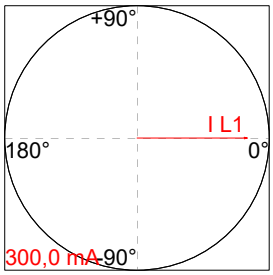
Title: Verificacion de Canal de Medida 25% Fase A

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	250,0 mA	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,250A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Assessment

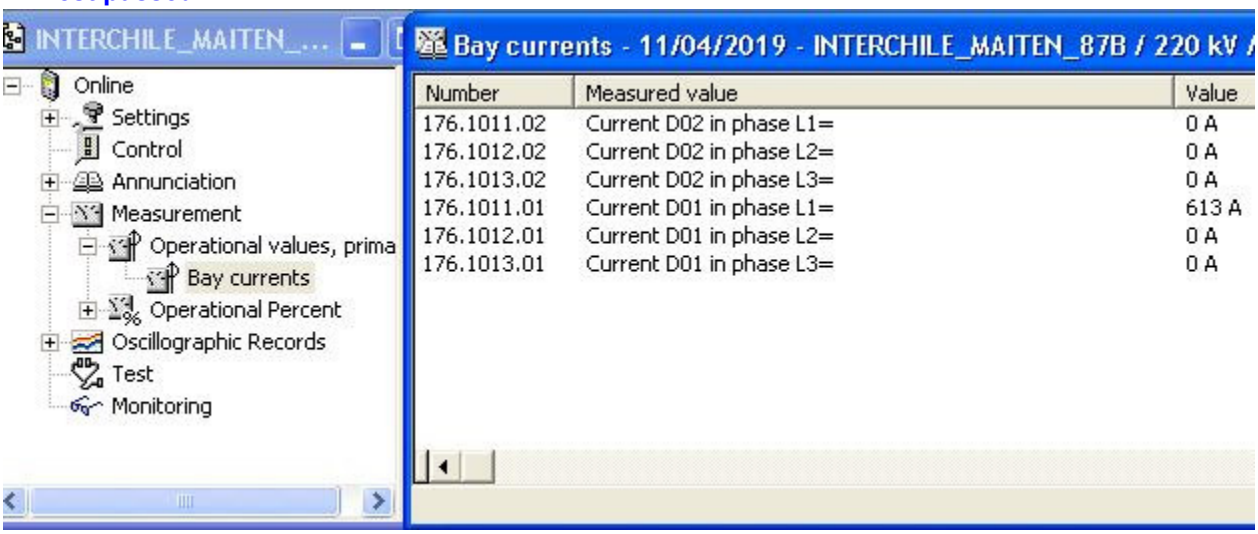
Passed 11-abr.-2019 02:48:44

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



2.2 Inyeccion 50% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:50:09	Test End:	11-abr.-2019 02:50:47
User Name:		Manager:	
Company:			

Test Results

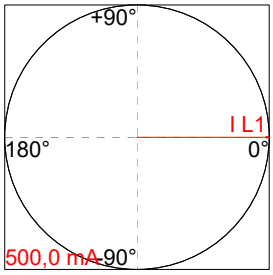
Title: Verificacion de Medida al 50% Fase A

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	500,0 mA	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,500A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Assessment

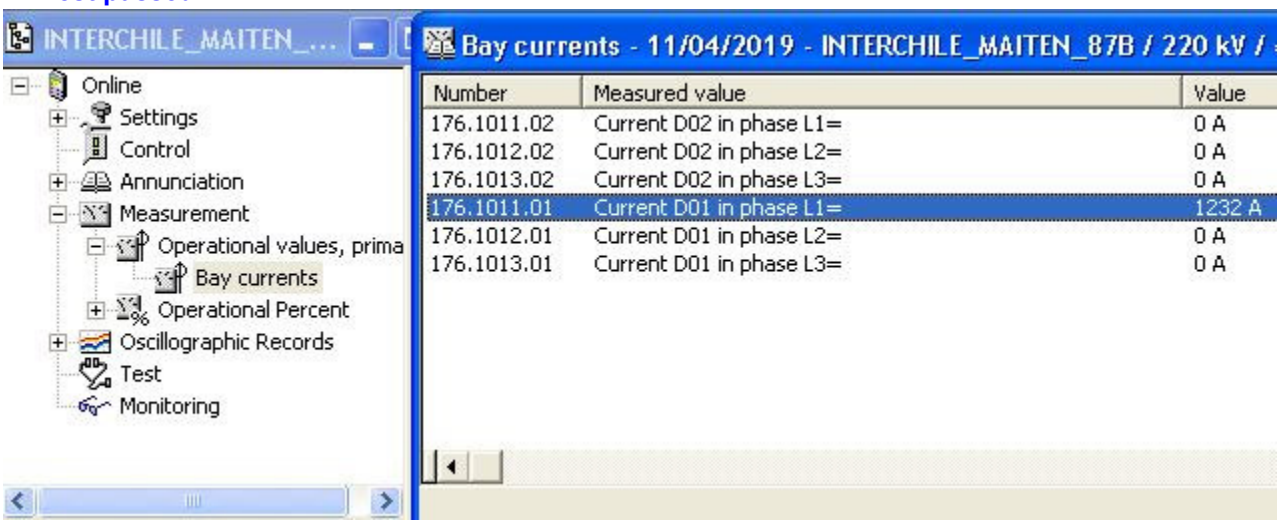
Passed 11-abr.-2019 02:50:12

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



2.3 Inyeccion 100% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation: NUEVA MAITENSILLO Substation address: 14
Bay: 52J2 Bay address:

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:50:52	Test End:	11-abr.-2019 02:51:23
User Name:		Manager:	
Company:			

Test Results

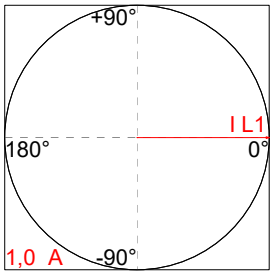
Title: Verificacion de Medida al 100% Fase A

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	1,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	1,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Assessment

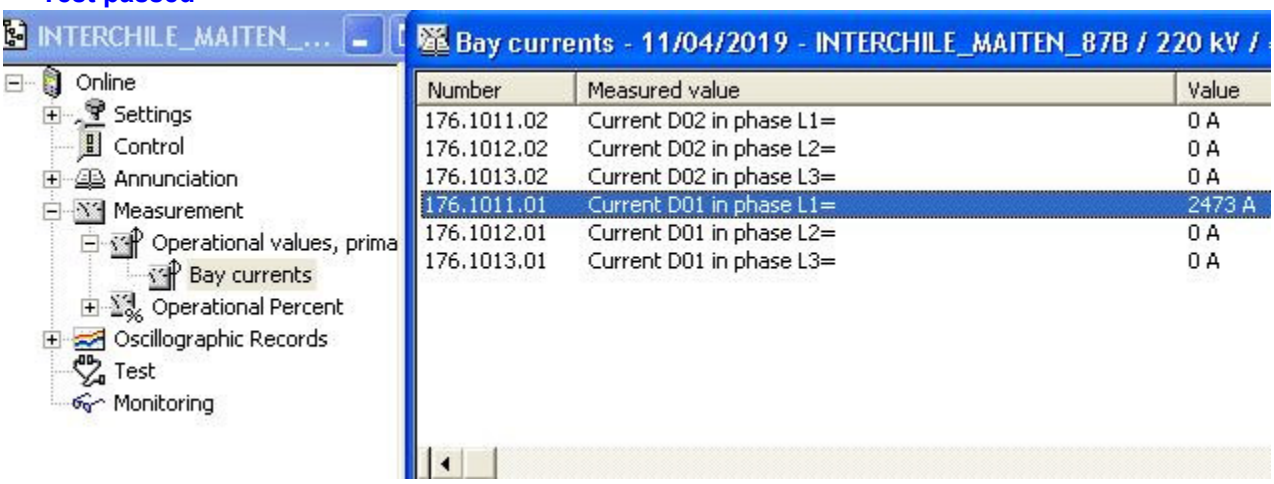
Passed 11-abr.-2019 02:50:55

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:1. Verificacion Medida Fase L1

Group:2. Verificacion Medida Fase L2

2.1 Inyeccion 25% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:51:30	Test End:	11-abr.-2019 02:52:14
User Name:		Manager:	
Company:			

Test Results

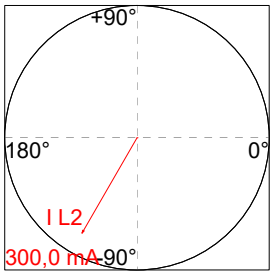
Title: Verificacion Medida al 25% Fase B

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	250,0 mA	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,250A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

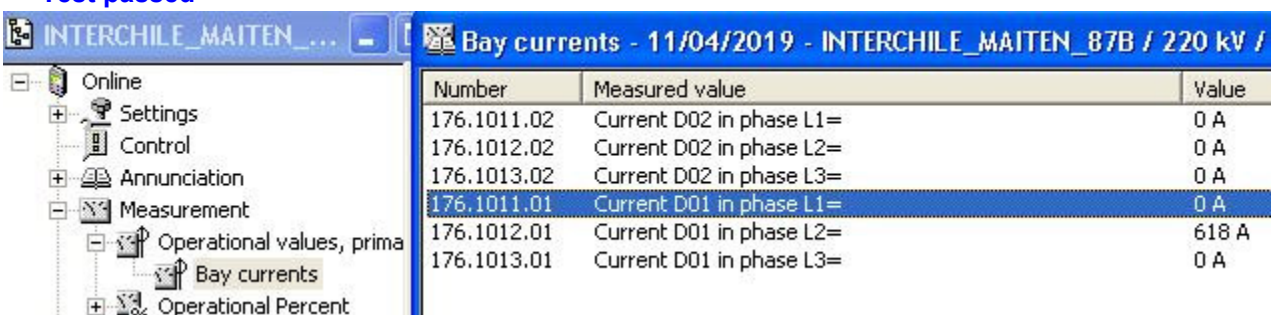
Passed 11-abr.-2019 02:51:40

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



2.2 Inyeccion 50% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:52:23	Test End:	11-abr.-2019 02:53:03
User Name:		Manager:	
Company:			

Test Results

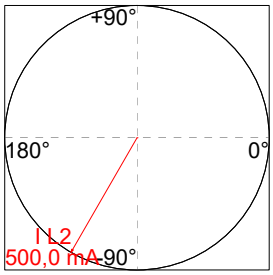
Title: Verificacion de Medidas al 50% Fase B

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	500,0 mA	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,500A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

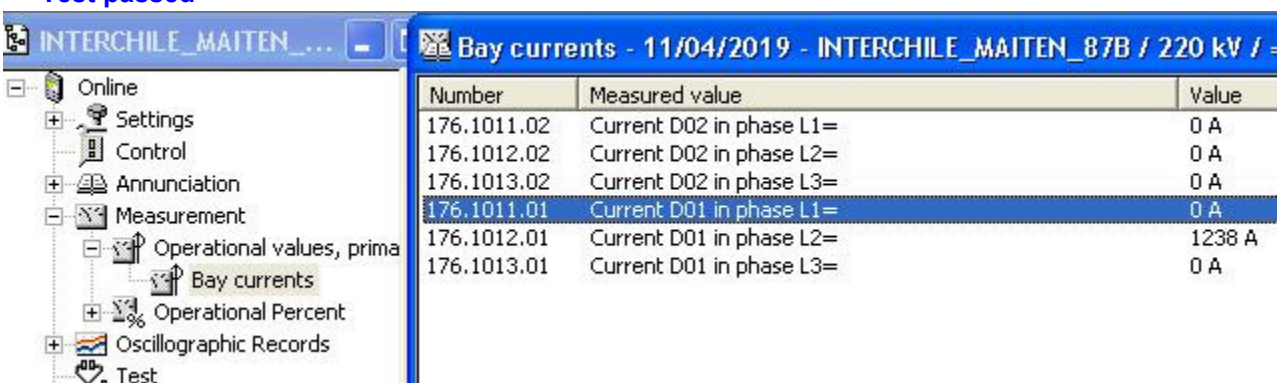
Passed 11-abr.-2019 02:52:29

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



2.3 Inyeccion 100% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:53:12	Test End:	11-abr.-2019 02:54:00
User Name:		Manager:	
Company:			

Test Results

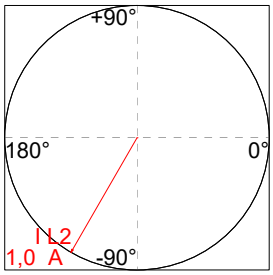
Title: Verificacion de Medidas al 100% Fase B

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	1,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	1,000A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

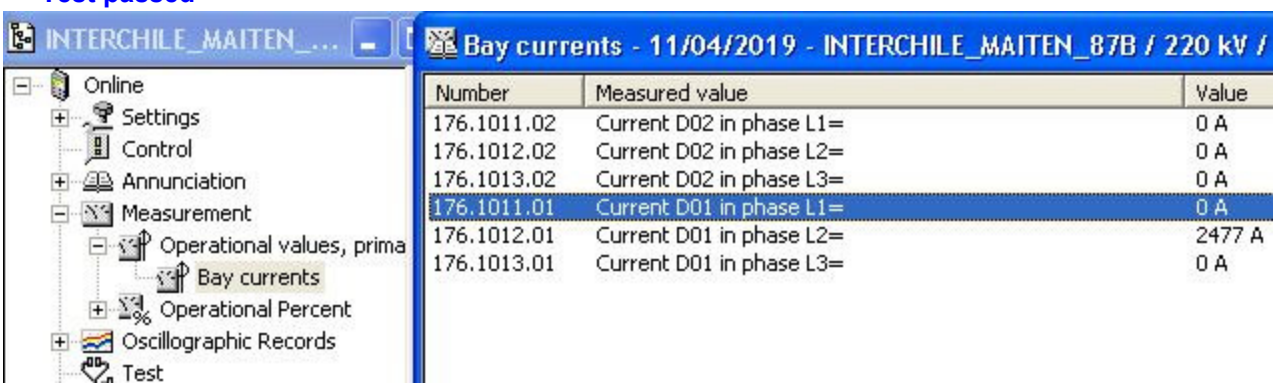
Passed 11-abr.-2019 02:53:17

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:2. Verificacion Medida Fase L2

Group:3. Verificacion Medida Fase L3

3.1 Inyeccion 25% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:54:25	Test End:	11-abr.-2019 02:54:59
User Name:		Manager:	
Company:			

Test Results

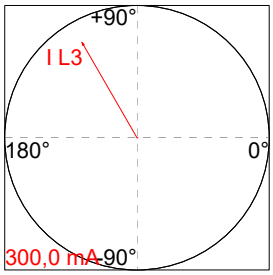
Title: Verificacion de Medidas al 25% Fase C

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	250,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,250A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

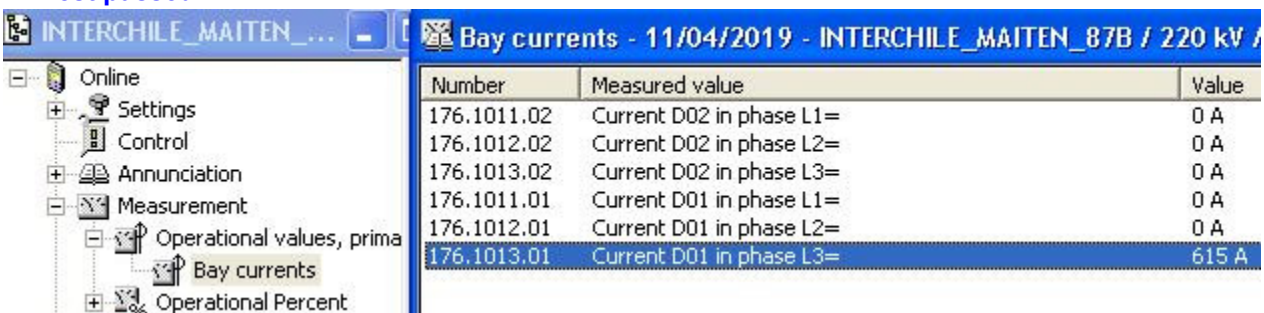
Passed 11-abr.-2019 02:54:28

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



3.2 Inyeccion 50% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:55:04	Test End:	11-abr.-2019 02:55:40
User Name:		Manager:	
Company:			

Test Results

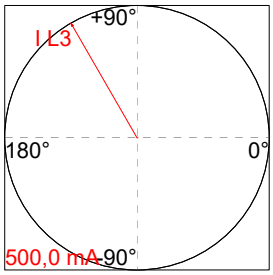
Title: Verificacion de Medidas al 50% Fase C

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	500,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,500A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

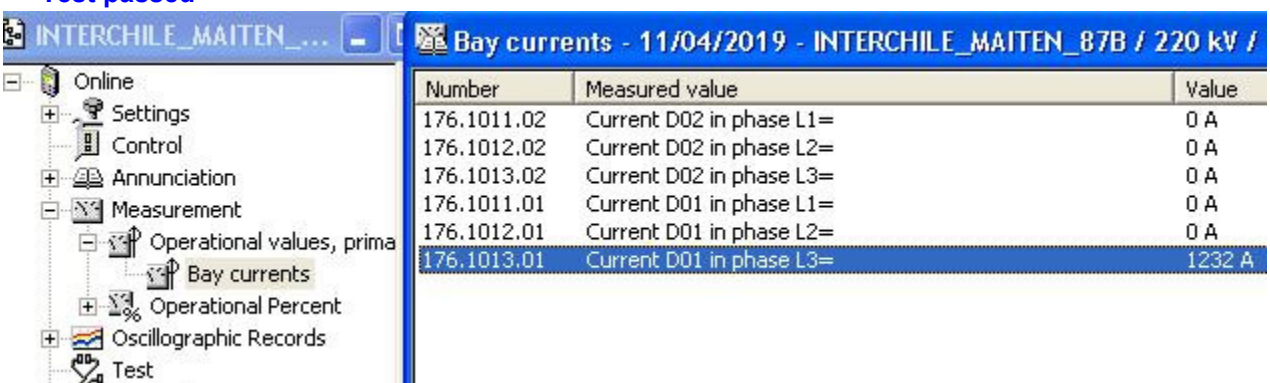
Passed 11-abr.-2019 02:55:13

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



3.3 Inyeccion 100% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:55:45	Test End:	11-abr.-2019 02:56:18
User Name:		Manager:	
Company:			

Test Results

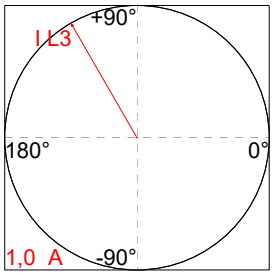
Title: Verificacion de medida al 100% Fase C

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	1,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	1,000A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

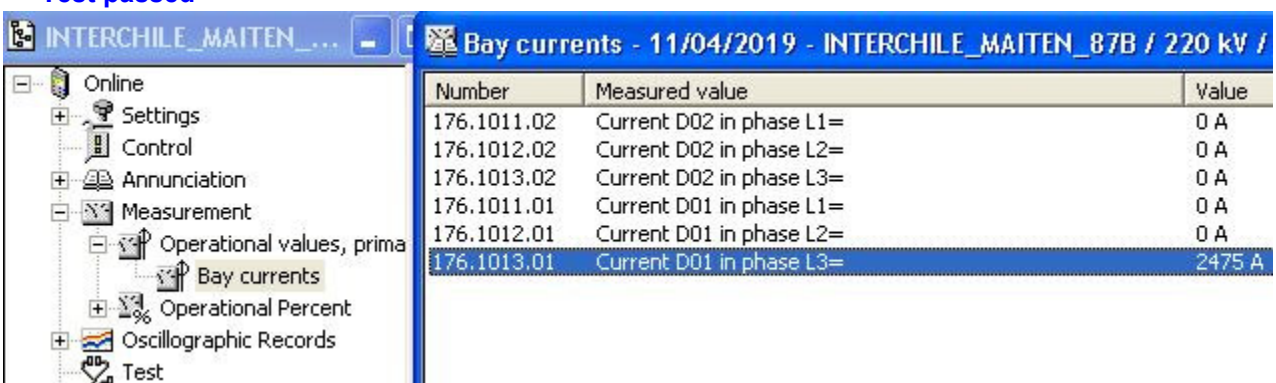
Passed 11-abr.-2019 02:55:50

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:3. Verificacion Medida Fase L3

Group:4. Verificacion Medida Fases L123

4.1 Inyeccion 25% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:56:25	Test End:	11-abr.-2019 02:57:00
User Name:		Manager:	
Company:			

Test Results

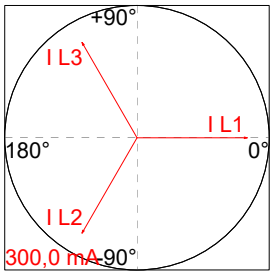
Title: Verificacion de Medidas al 25% Fase ABC

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	250,0 mA	0,00 °	50,000 Hz
	I L2	250,0 mA	-120,00 °	50,000 Hz
	I L3	250,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,250A	0,00°
I L2	0,250A	-120,00°
I L3	0,250A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

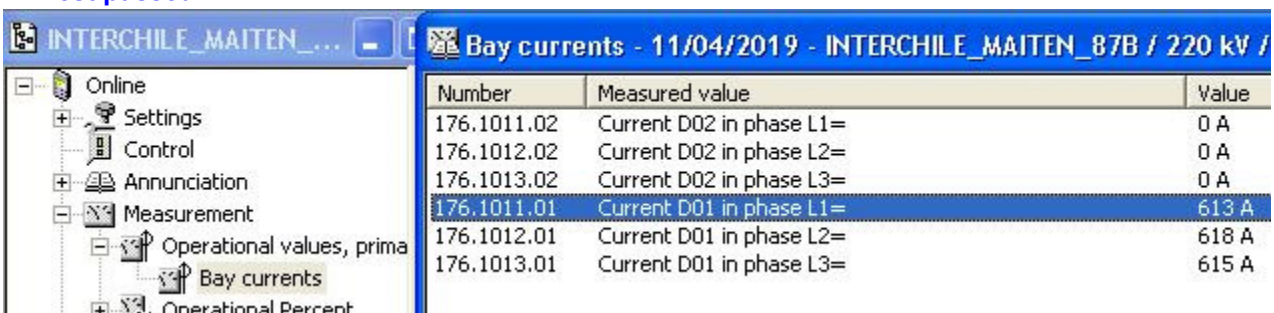
Passed 11-abr.-2019 02:56:29

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



4.2 Inyeccion 50% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:57:05	Test End:	11-abr.-2019 02:57:40
User Name:		Manager:	
Company:			

Test Results

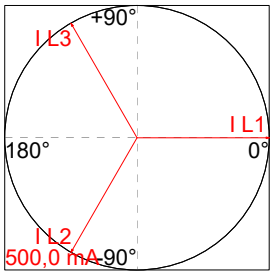
Title: Verificacion de Medidas al 50% Fase ABC

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	500,0 mA	0,00 °	50,000 Hz
	I L2	500,0 mA	-120,00 °	50,000 Hz
	I L3	500,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,500A	0,00°
I L2	0,500A	-120,00°
I L3	0,500A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
ENVIO DDT	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

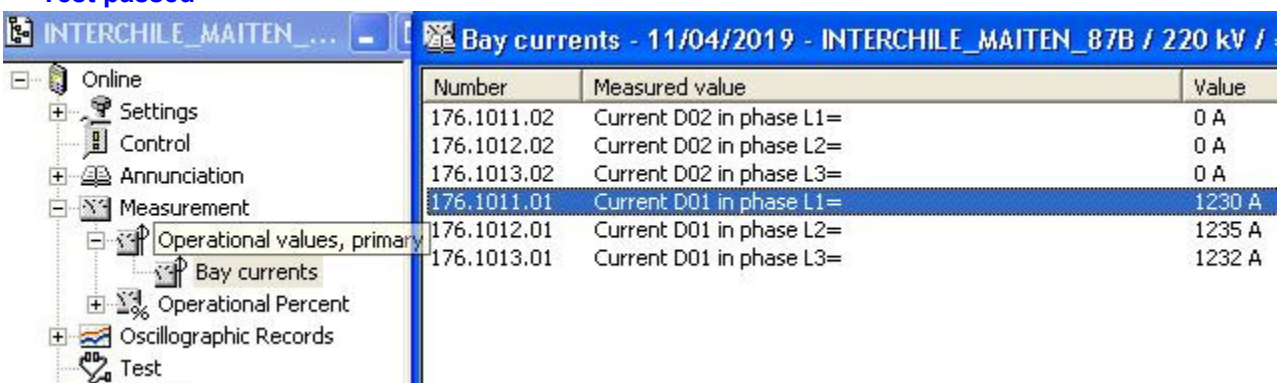
Passed 11-abr.-2019 02:57:14

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



4.3 Inyeccion 100% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 02:57:46	Test End:	11-abr.-2019 02:58:18
User Name:		Manager:	
Company:			

Test Results

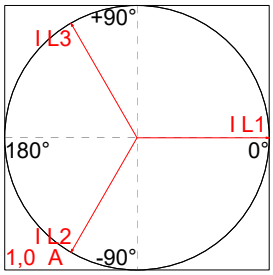
Title: Verificacion de Medidas al 100% Fase ABC

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	1,000 A	0,00 °	50,000 Hz
	I L2	1,000 A	-120,00 °	50,000 Hz
	I L3	1,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	1,000A	0,00°
I L2	1,000A	-120,00°
I L3	1,000A	120,00°



Binary Outputs

Name	State
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

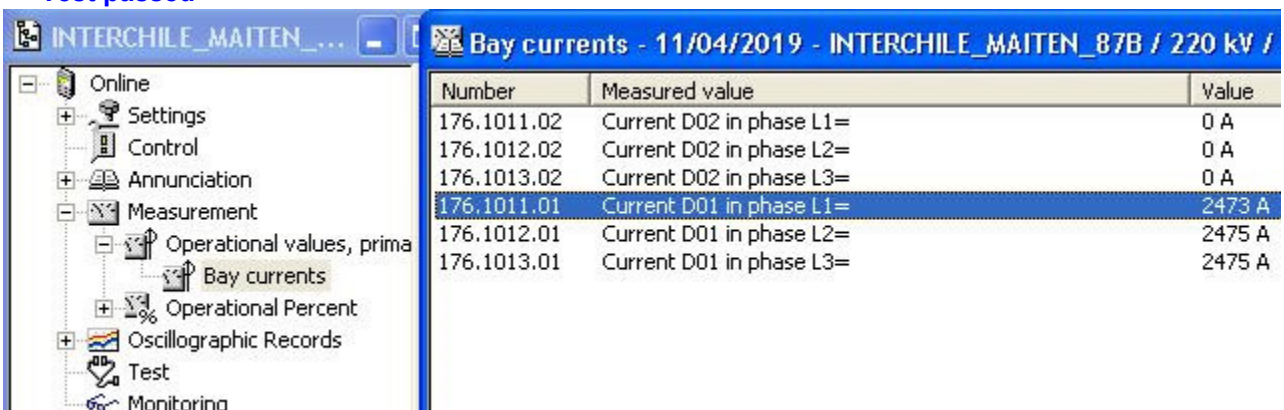
Passed 11-abr.-2019 02:57:50

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:4. Verificacion Medida Fases L123

Group:5. Verificacion Pickup 50BF Fase L1

6.1 Pickup con Arranque Fase L1:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	1
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	OR
TRIP 87B-L1	1
TRIP 87B-L2	X
TRIP 87B-L3	X
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	X
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 03:00:13
Test End: 11-abr.-2019 03:00:21
User Name:
Manager:
Company:

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L1	Ramp 1	TRIP 87B-L1 0->1	I L1	100,0 mA	105,0 mA	300,0 mA	300,0 mA	5,000 mA	+	69,60 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

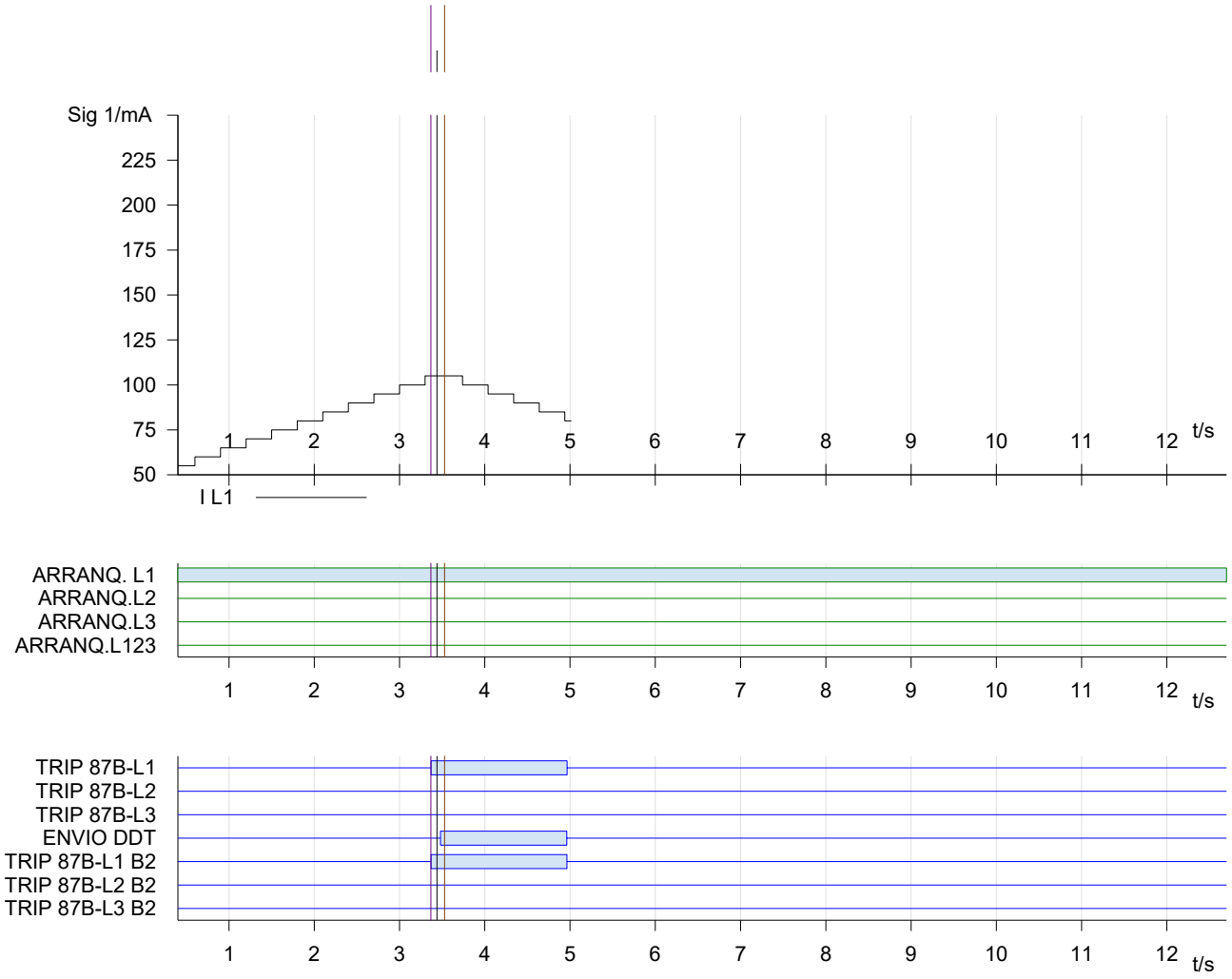
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
Drop-off/Pick-up	X/Y	Pickup_Fase L1	Pickup_Fase L1	0,9500	1,000			0,05000	+

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	3,368 s	<none>	n/a
Cursor 2	3,528 s	<none>	n/a
C2 - C1	160,4 ms		n/a

Test State:
Test passed

6.2 Pickup sin Arranque Fase L1:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	OR
TRIP 87B-L1	1
TRIP 87B-L2	X
TRIP 87B-L3	X
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	X
Step back	Yes

Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 03:00:34	Test End:	11-abr.-2019 03:00:43
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

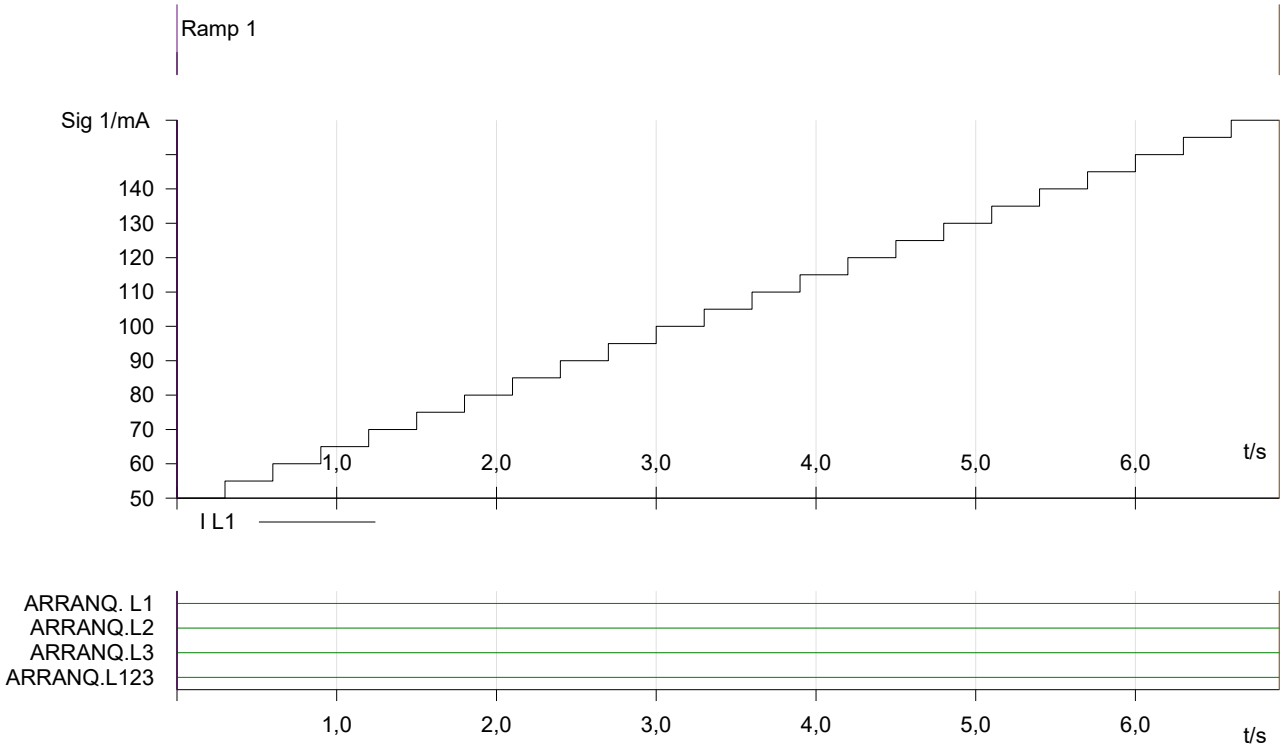
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

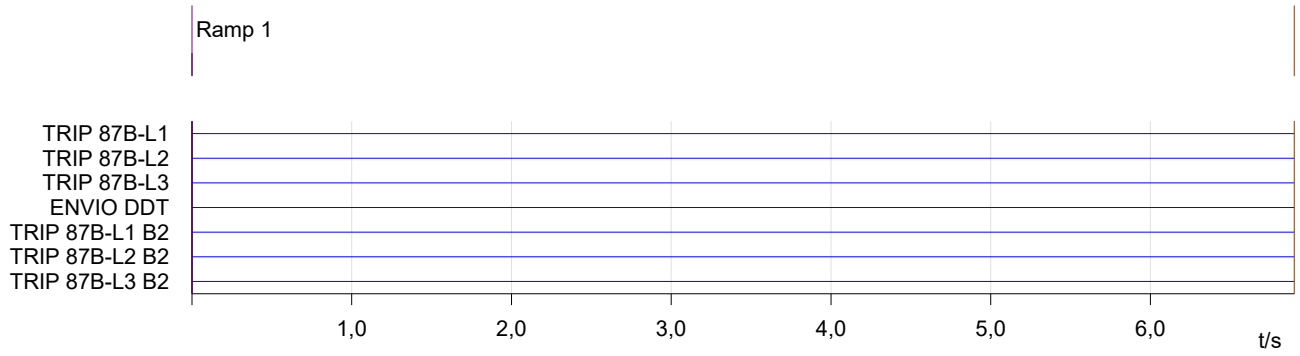
Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	6,900 s	<none>	n/a
C2 - C1	6,900 s		n/a

Test State:
Test passed

Group end:5. Verificacion Pickup 50BF Fase L1

Group:7. Verificacion Pickup 50BF Fase L2

7.1 Pickup con Arranque Fase L2:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s

ARRANQ. L1	0
ARRANQ.L2	1
ARRANQ.L3	0
ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	X
TRIP 87B-L2	1
TRIP 87B-L3	X
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	X
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 03:01:24	Test End:	11-abr.-2019 03:01:31
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	TRIP 87B-L2 0->1 and TRIP 87B-L2 B2 0->1	I L2	100,0 mA	105,0 mA	300,0 mA	300,0 mA	5,000 mA	+	62,10 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

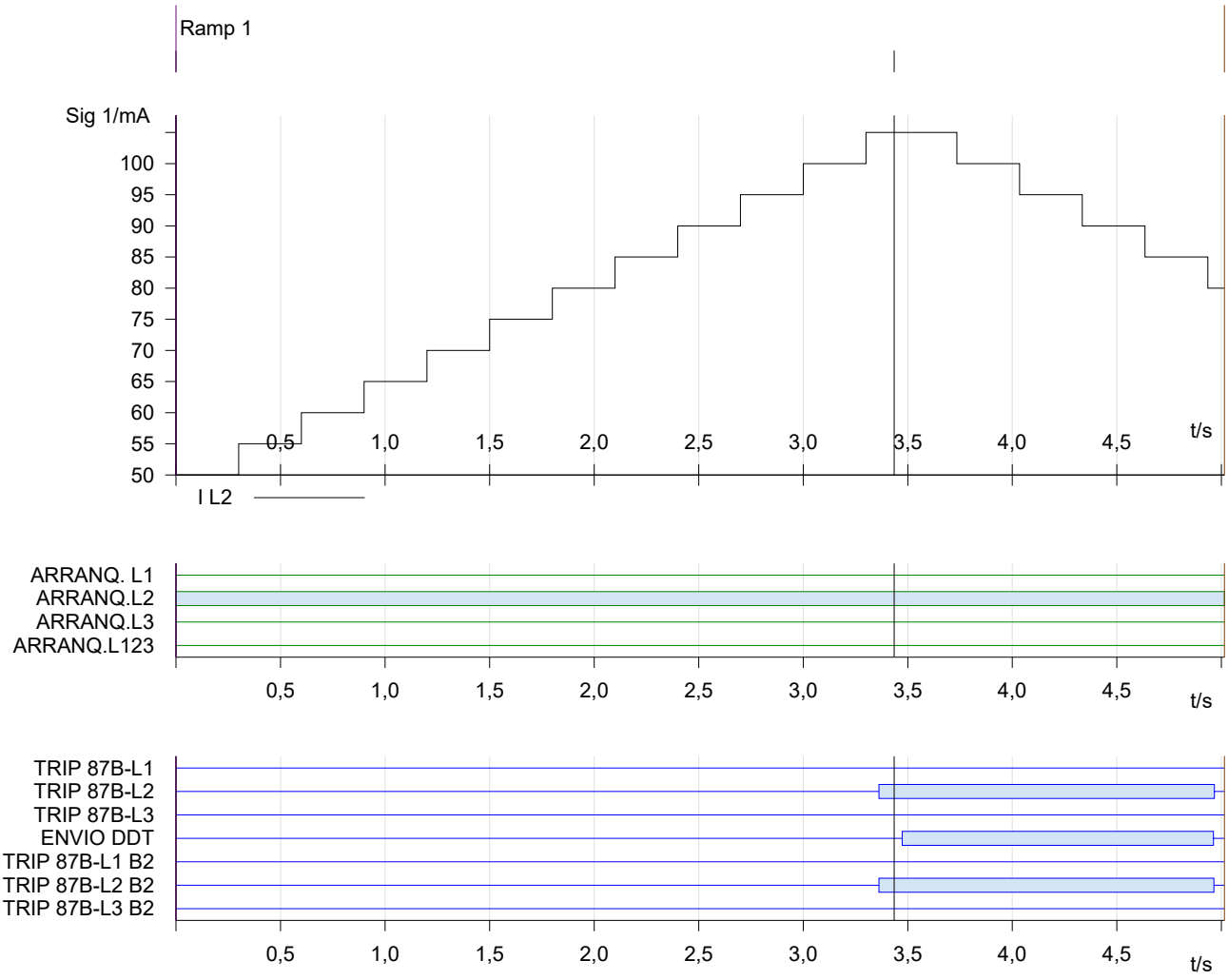
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
Drop-off/Pick-up	X/Y	Pickup_Fase L2	Pickup_Fase L2	0,9500	1,000			0,05000	+

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	5,014 s	<none>	n/a
C2 - C1	5,014 s		n/a

Test State:

Test passed

7.2 Pickup sin Arranque Fase L2:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	X
TRIP 87B-L2	1
TRIP 87B-L3	X
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 03:01:47	Test End:	11-abr.-2019 03:01:56
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

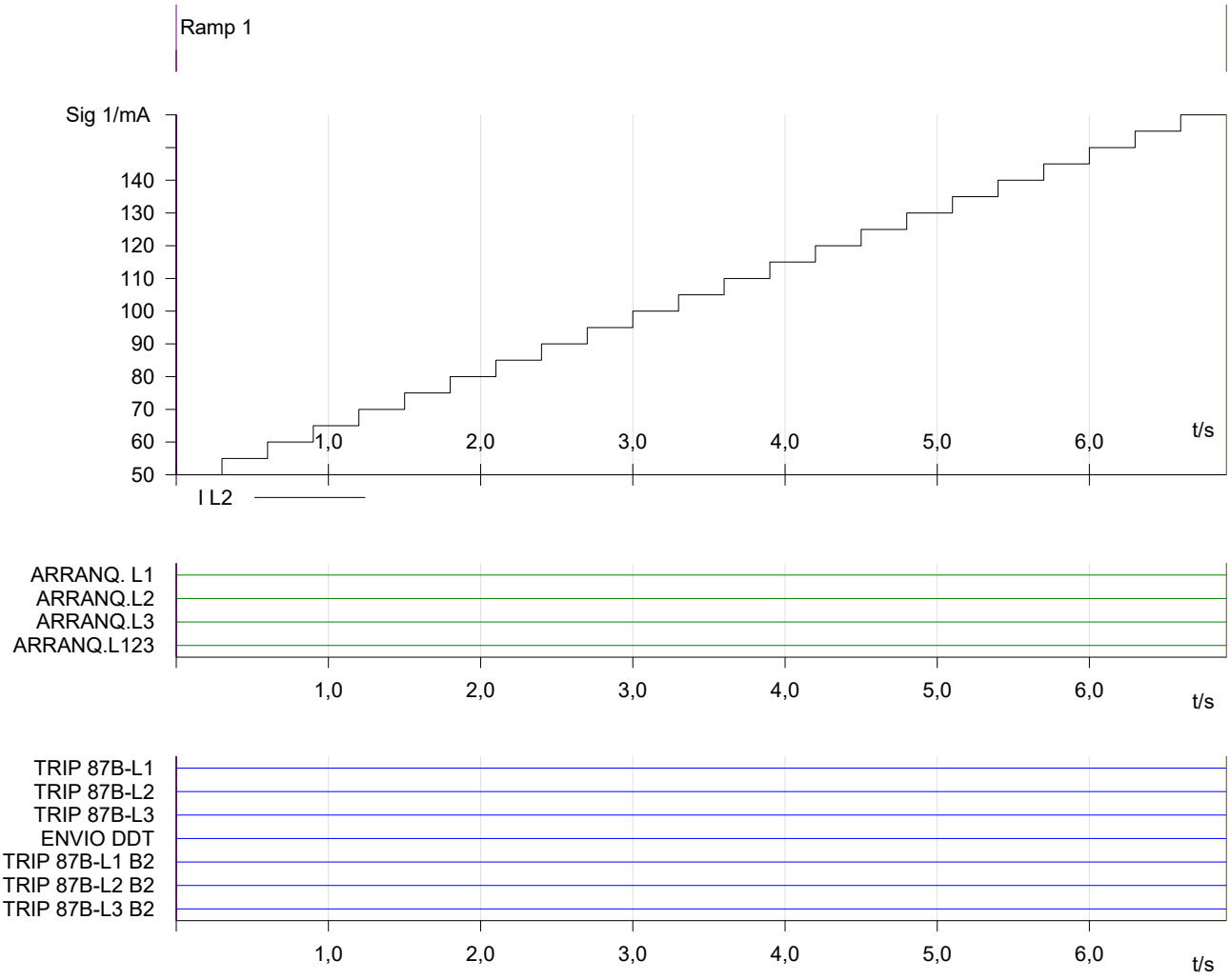
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	6,900 s	<none>	n/a
C2 - C1	6,900 s		n/a

Test State:
Test passed

- Group end:7. Verificacion Pickup 50BF Fase L2 -
- Group:8. Verificacion Pickup 50BF Fase L3 -

8.1 Pickup con Arranque Fase L3:

Test Settings

General

No. of ramp states:	1
Total steps per test:	23
Total time per test:	6,900 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	1
ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	X
TRIP 87B-L2	X
TRIP 87B-L3	1
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 03:03:00	Test End:	11-abr.-2019 03:03:07
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	TRIP 87B-L3 0->1 and TRIP 87B-L3 B2 0->1	I L3	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	75,50 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

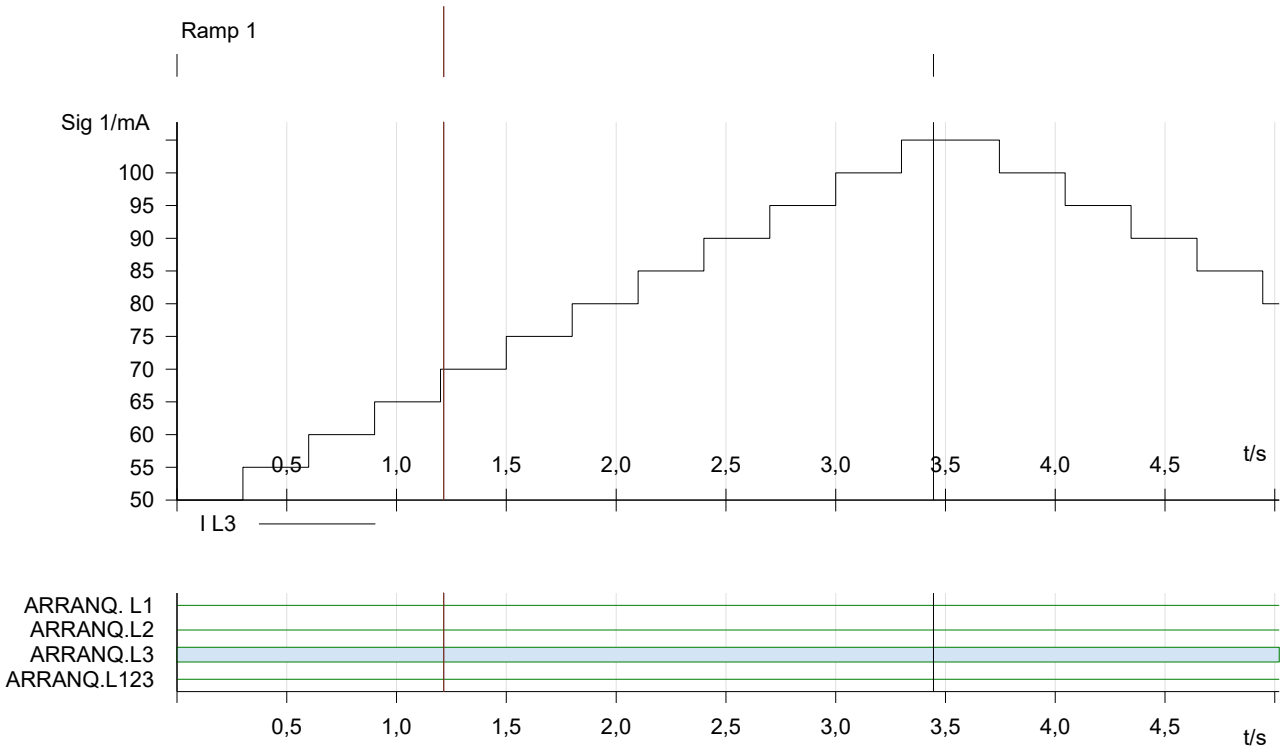
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
Drop-off/Pick-up	X/Y	Pickup_Fase L2	Pickup_Fase L2	0,9500	1,000			0,05000	+

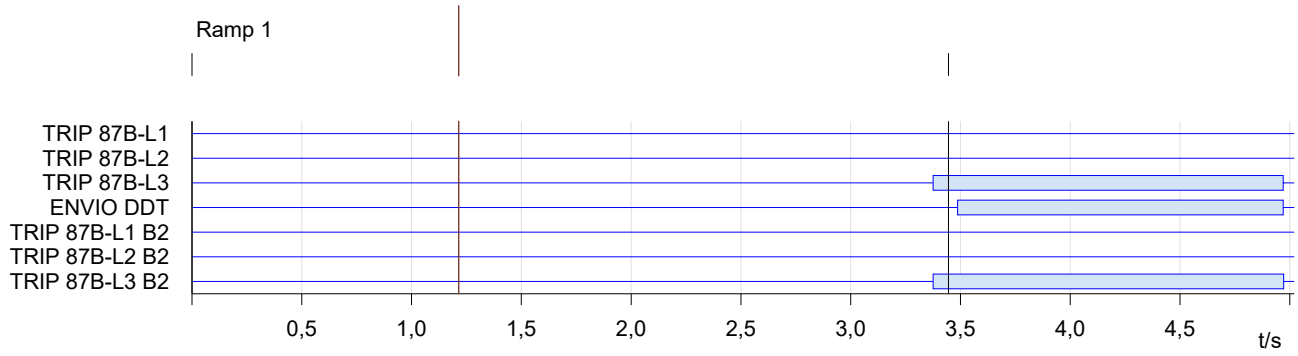
Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

	Time	Signal	Value
Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:
Test passed

8.2 Pickup sin Arranque Fase L3:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0

ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	X
TRIP 87B-L2	X
TRIP 87B-L3	1
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 03:03:28	Test End:	11-abr.-2019 03:03:37
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

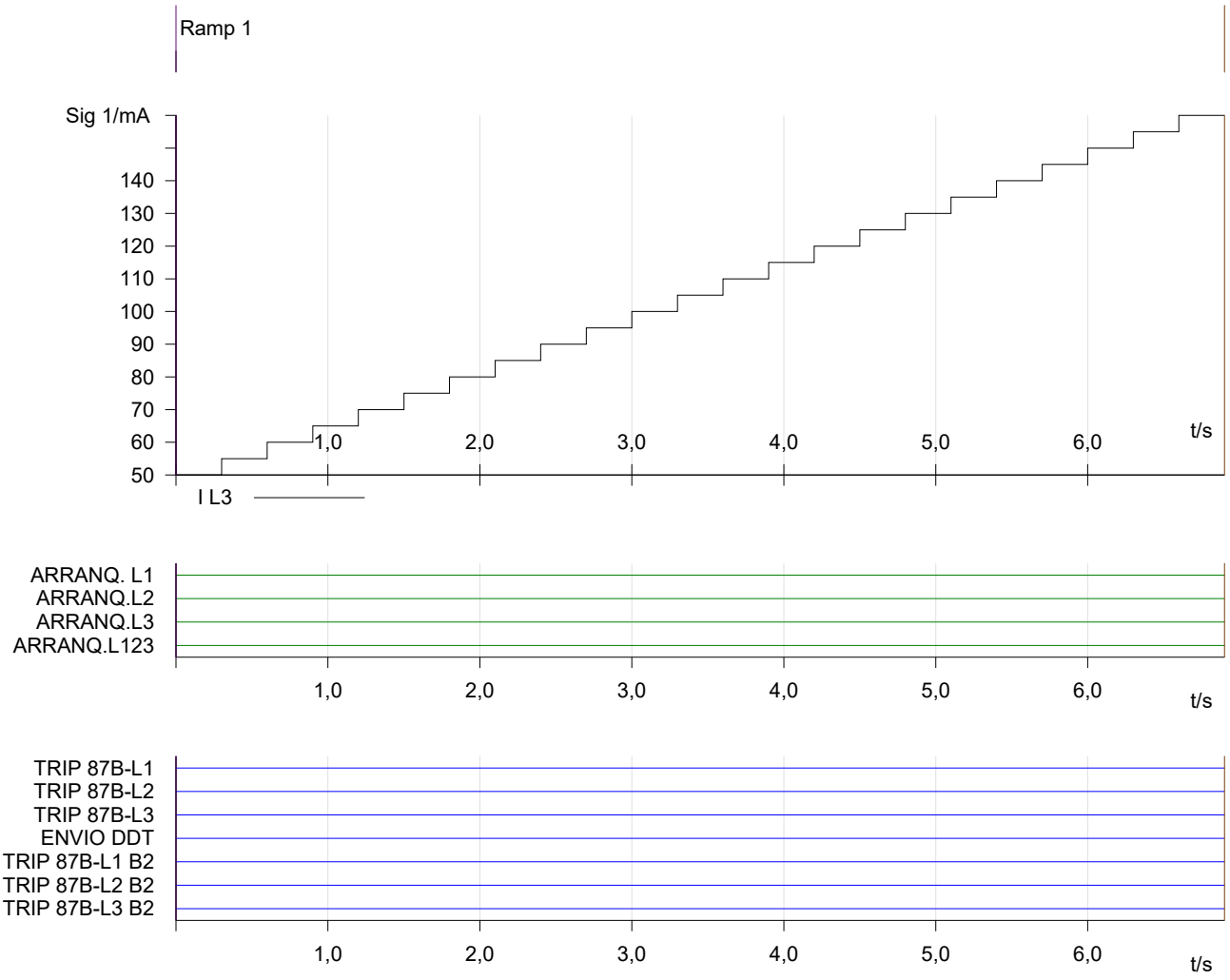
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	6,900 s	<none>	n/a
C2 - C1	6,900 s		n/a

Test State:

Test passed

Group end:8. Verificacion Pickup 50BF Fase L3

Group:9. Verificacion Pickup 50BF Fases L123

8.1 Pickup con Arranque Fases L123:

Test Settings

General

No. of ramp states:	1
Total steps per test:	23
Total time per test:	6,900 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	1
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	1
TRIP 87B-L2	1
TRIP 87B-L3	1
ENVIO DDT	X
TRIP 87B-L1 B2	1
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 03:04:31	Test End:	11-abr.-2019 03:04:38
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L123	Ramp 1	TRIP 87B-L3 0->1 and TRIP 87B-L1 B2 0->1 and TRIP 87B-L1 0->1 and TRIP 87B-L2 0->1 and TRIP 87B-L2 B2 0->1 and TRIP 87B-L3 B2 0->1	I L1; L2; L3	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	17,90 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

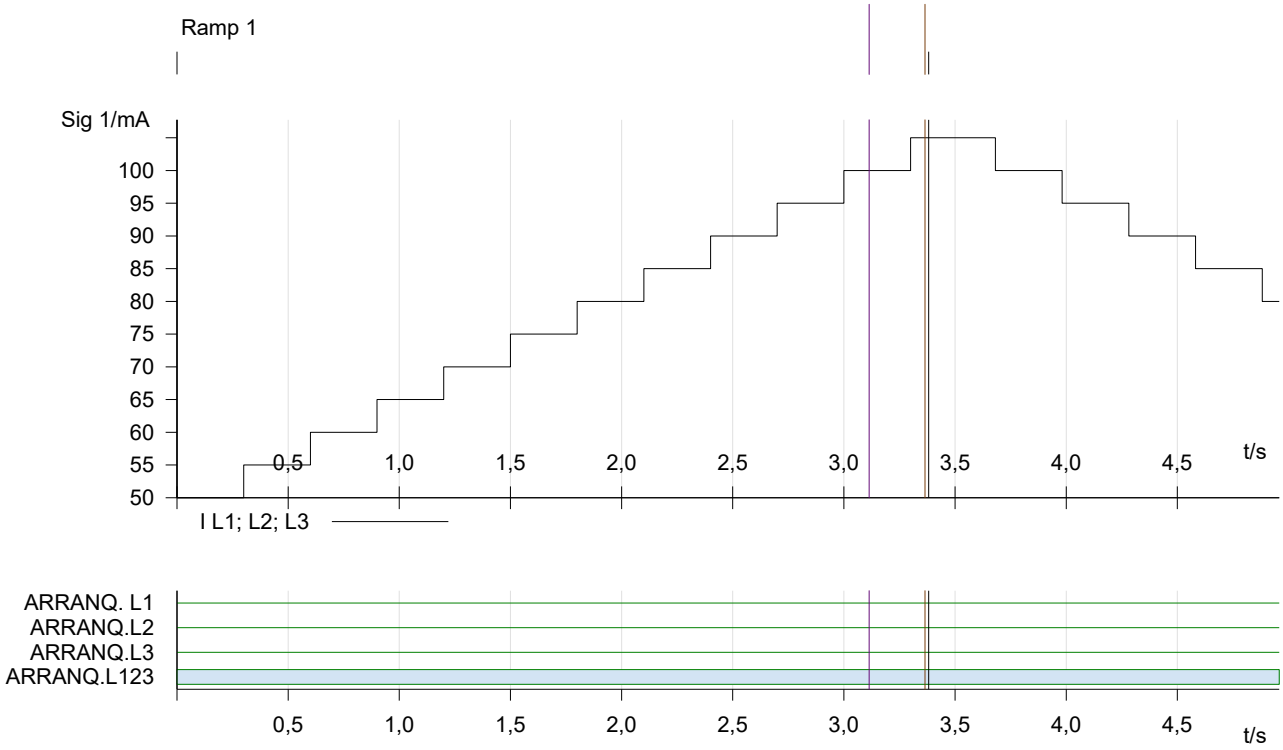
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

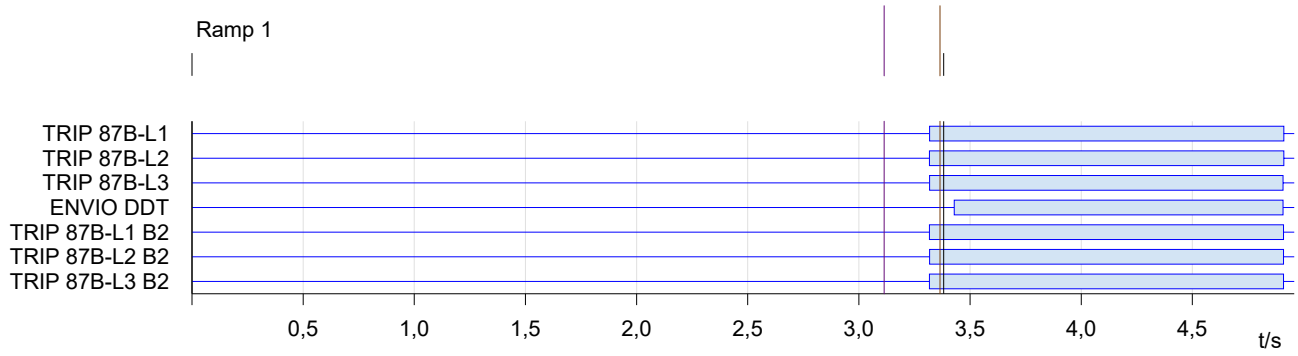
Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

	Time	Signal	Value
Cursor 1	3,113 s	<none>	n/a
Cursor 2	3,365 s	<none>	n/a
C2 - C1	251,4 ms		n/a

Test State:
Test passed

8.2 Pickup sin Arranque Fases L123:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From **Sig 1 To** **Sig 1 Delta** **Sig 1 d/dt**	50,00 mA 160,0 mA 5,000 mA 16,67 mA/s
ARRANQ. L1 **ARRANQ.L2** **ARRANQ.L3**	0 0 0

ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	1
TRIP 87B-L2	1
TRIP 87B-L3	1
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	X
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 03:04:55	Test End:	11-abr.-2019 03:05:04
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

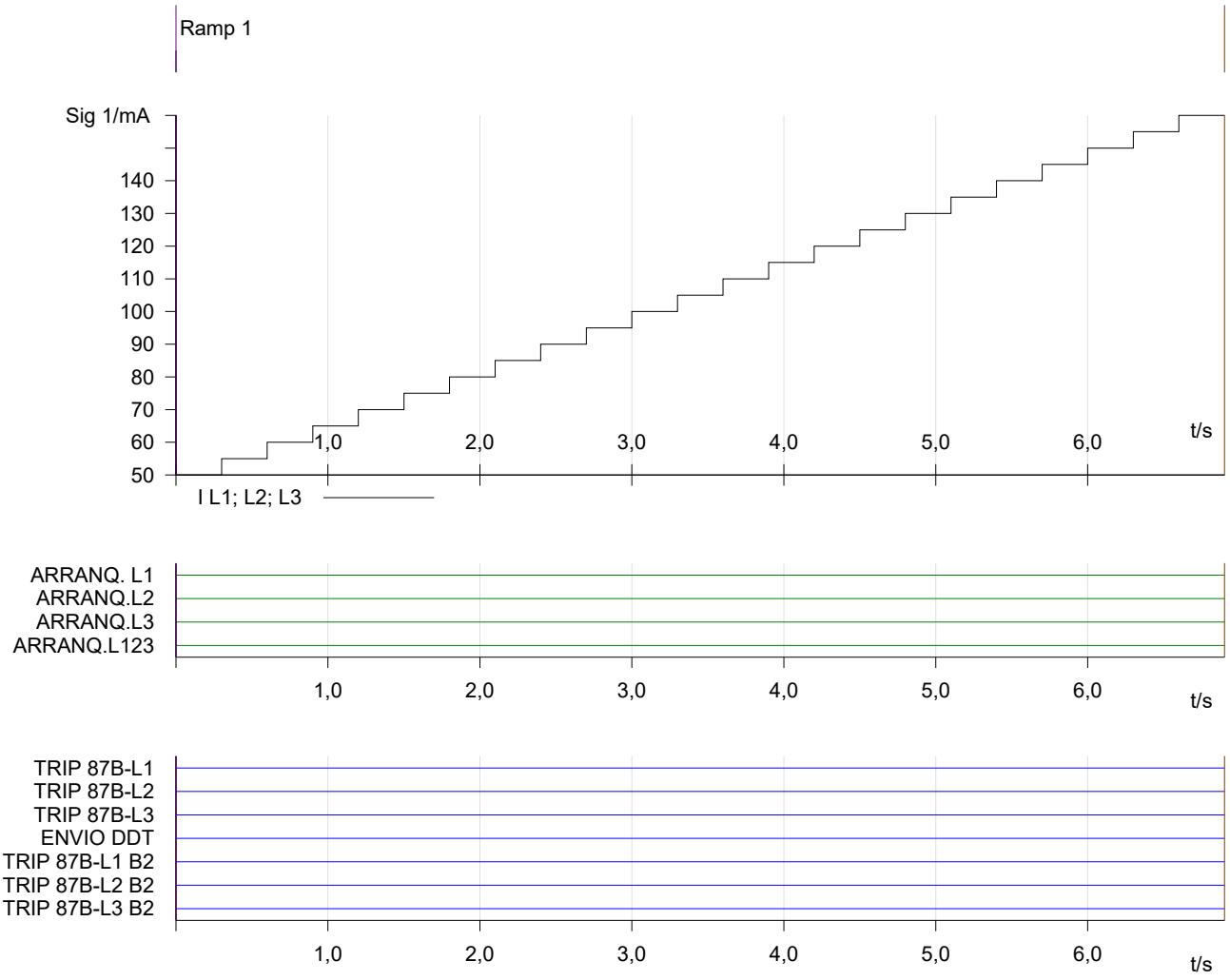
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	6,900 s	<none>	n/a
C2 - C1	6,900 s		n/a

Test State:

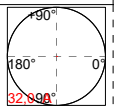
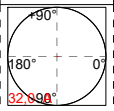
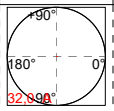
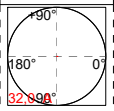
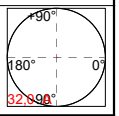
Test passed

Group end:9. Verificacion Pickup 50BF Fases L123

Group:10. Operacion 50BF_J2 (T1)

9.1 Operacion 50BF_Fase L1 :

Test Settings

State	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1	Post-Falla 2
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	1	0
ARRANQ.L2	0	0	0	0	0
ARRANQ.L3	0	0	0	0	0
ARRANQ.L123	0	0	0	0	0
Max. State Time	3,000 s	3,000 s	1,000 s	100,0 ms	1,000 s
Trigger Logic				AND	OR
TRIP 87B-L1				1	1
TRIP 87B-L2				0	X
TRIP 87B-L3				0	X
TRIP 87B-L1 B2				1	X
User interaction	no	no	no	no	no
CMGPS trigger	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no
Pulses / seconds	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	50,00 ms	0,000 s
On trigger jump to test end	no	no	no	no	no
Diagrams					

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:07:59	Test End:	11-abr.-2019 03:08:07
User Name:		Manager:	
Company:			

Test Results

Time Assessment

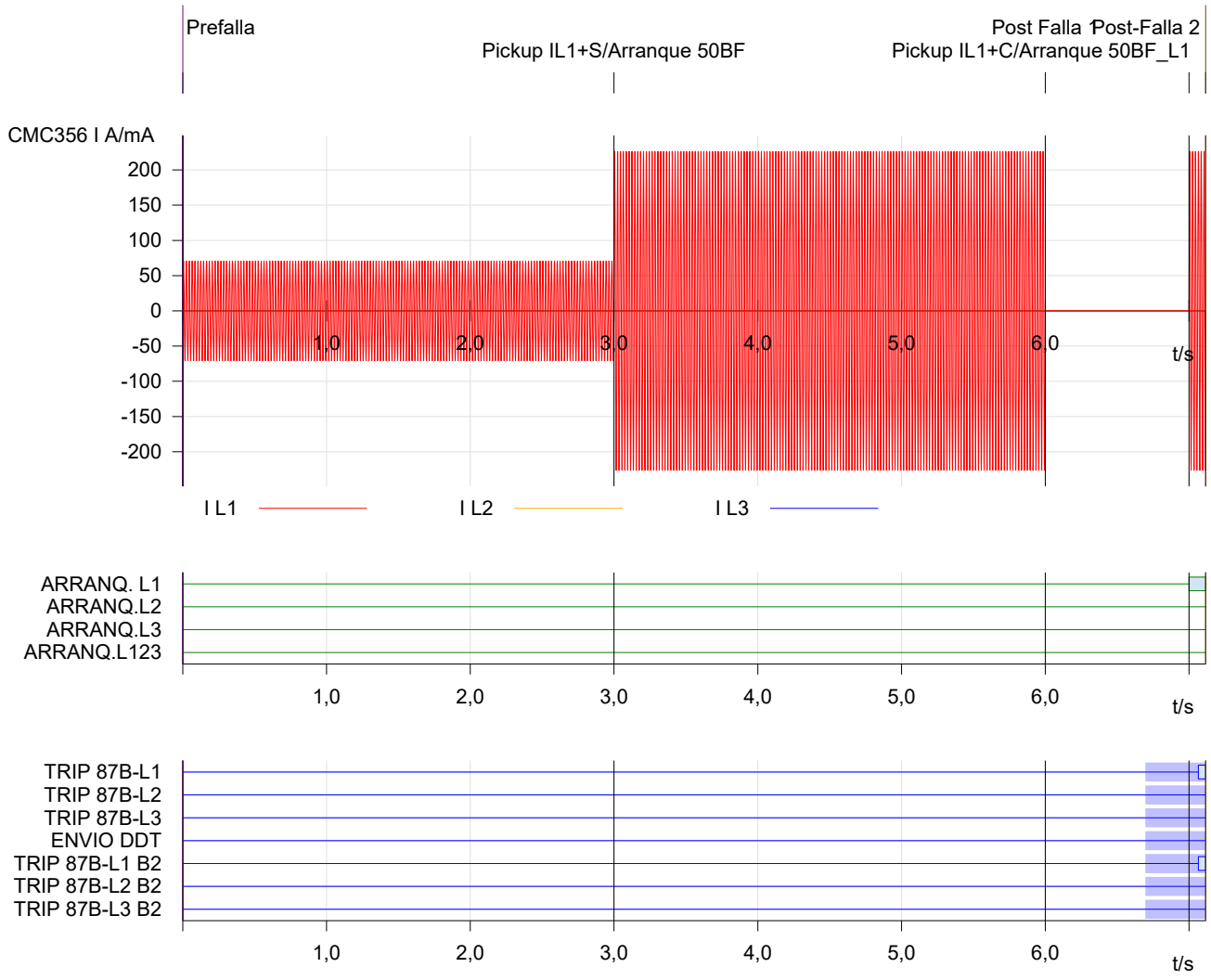
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	TRIP 87B-L1 0>1	50,00 ms	30,00 ms	30,00 ms	65,70 ms	15,70 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1	Post-Falla 2
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	50,00 ms
TRIP 87B-L1	0	0	0	1	0
TRIP 87B-L2	0	0	0	0	0
TRIP 87B-L3	0	0	0	0	0
ENVIO DDT	0	0	0	0	0
TRIP 87B-L1 B2	0	0	0	1	0
TRIP 87B-L2 B2	0	0	0	0	0
TRIP 87B-L3 B2	0	0	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

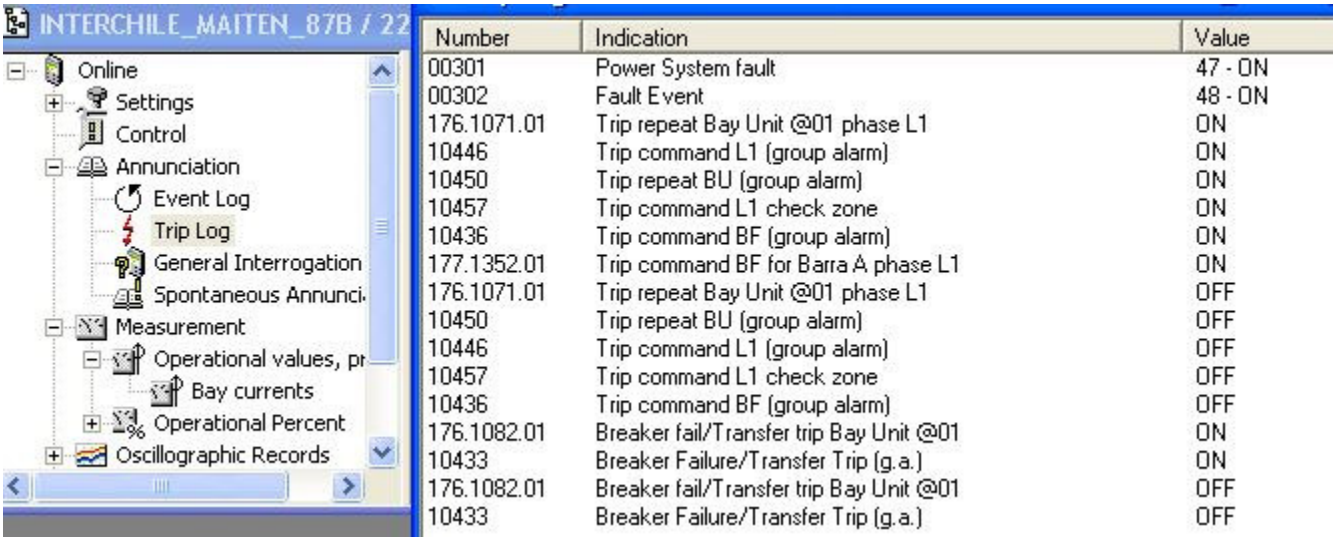
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,116 s	<none>	n/a
C2 - C1	7,116 s		n/a

Event recorder

Time	Type	Signal name	Slope
7,000 s	Output	ARRANQ. L1	0>1
7,065 s	Input	TRIP 87B-L1 B2	0>1
7,066 s	Input	TRIP 87B-L1	0>1
7,116 s	Output	ARRANQ. L1	1>0

Test State:

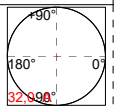
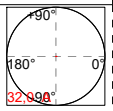
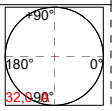
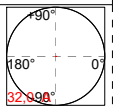
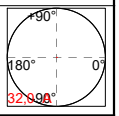
Test passed



9.2 Operacion 50BF_Fase L2 :

Test Settings

State	Prefalla	Pickup IL2+S/Arranque 50BF	Post Falla 1	Pickup IL2+C/Arranque 50BF_L2	Post-Falla 2
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

ARRANQ. L1	0	0	0	0	0
ARRANQ.L2	0	0	0	1	0
ARRANQ.L3	0	0	0	0	0
ARRANQ.L123	0	0	0	0	0
Max. State Time	3,000 s	2,000 s	100,0 ms	100,0 ms	1,000 s
Trigger Logic			OR	AND	
TRIP 87B-L2			1	1	
TRIP 87B-L2 B2			X	1	
User interaction	no	no	no	no	no
CMGPS trigger	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no
Pulses / seconds	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	yes	no	no
Diagrams					

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:11:54	Test End:	11-abr.-2019 03:12:01
User Name:		Manager:	
Company:			

Test Results

Time Assessment

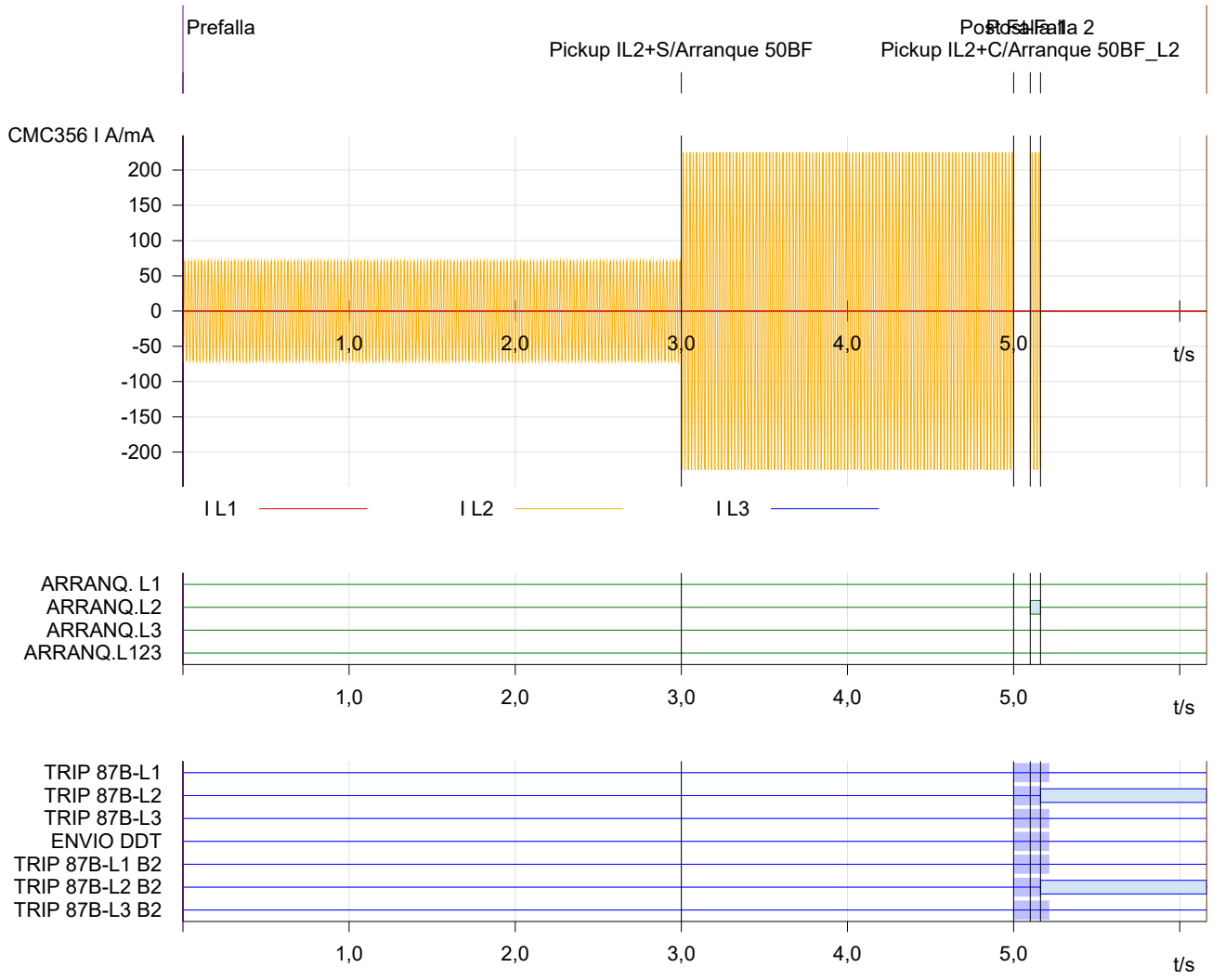
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	TRIP 87B-L2 0>1	50,00 ms	30,00 ms	30,00 ms	61,80 ms	11,80 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL2+S/Arranque 50BF	Post Falla 1	Pickup IL2+C/Arranque 50BF_L2	Post-Falla 2
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	50,00 ms
TRIP 87B-L1	0	0	0	0	0
TRIP 87B-L2	0	0	0	1	X
TRIP 87B-L3	0	0	0	0	0
ENVIO DDT	0	0	0	0	0
TRIP 87B-L1 B2	0	0	0	0	0
TRIP 87B-L2 B2	0	0	0	1	X
TRIP 87B-L3 B2	0	0	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

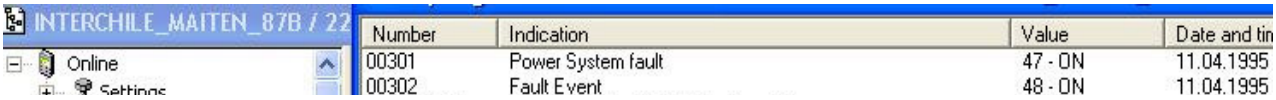
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	6,162 s	<none>	n/a
C2 - C1	6,162 s		n/a

Event recorder

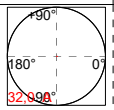
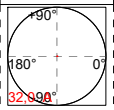
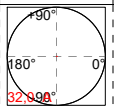
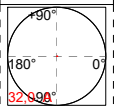
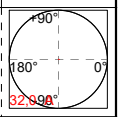
Time	Type	Signal name	Slope
5,100 s	Output	ARRANQ.L2	0>1
5,162 s	Input	TRIP 87B-L2	0>1
5,162 s	Input	TRIP 87B-L2 B2	0>1
5,162 s	Output	ARRANQ.L2	1>0
6,162 s	Input	TRIP 87B-L2	1>0
6,162 s	Input	TRIP 87B-L2 B2	1>0

Test State:

Test passed



Test Settings

State	Prefalla	Pickup IL3+S/Arranque 50BF	Post Falla 1	Pickup IL3+C/Arranque 50BF_L3	Post-Falla 2
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	0	0
ARRANQ.L2	0	0	0	0	0
ARRANQ.L3	0	0	0	1	0
ARRANQ.L123	0	0	0	0	0
Max. State Time	3,000 s	2,000 s	1,000 s	100,0 ms	1,000 s
Trigger Logic				AND	
TRIP 87B-L3				1	
TRIP 87B-L3 B2				1	
User interaction	no	no	no	no	no
CMGPS trigger	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no
Pulses / seconds	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no
Diagrams					

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:14:29	Test End:	11-abr.-2019 03:14:38
User Name:		Manager:	
Company:			

Test Results

Time Assessment

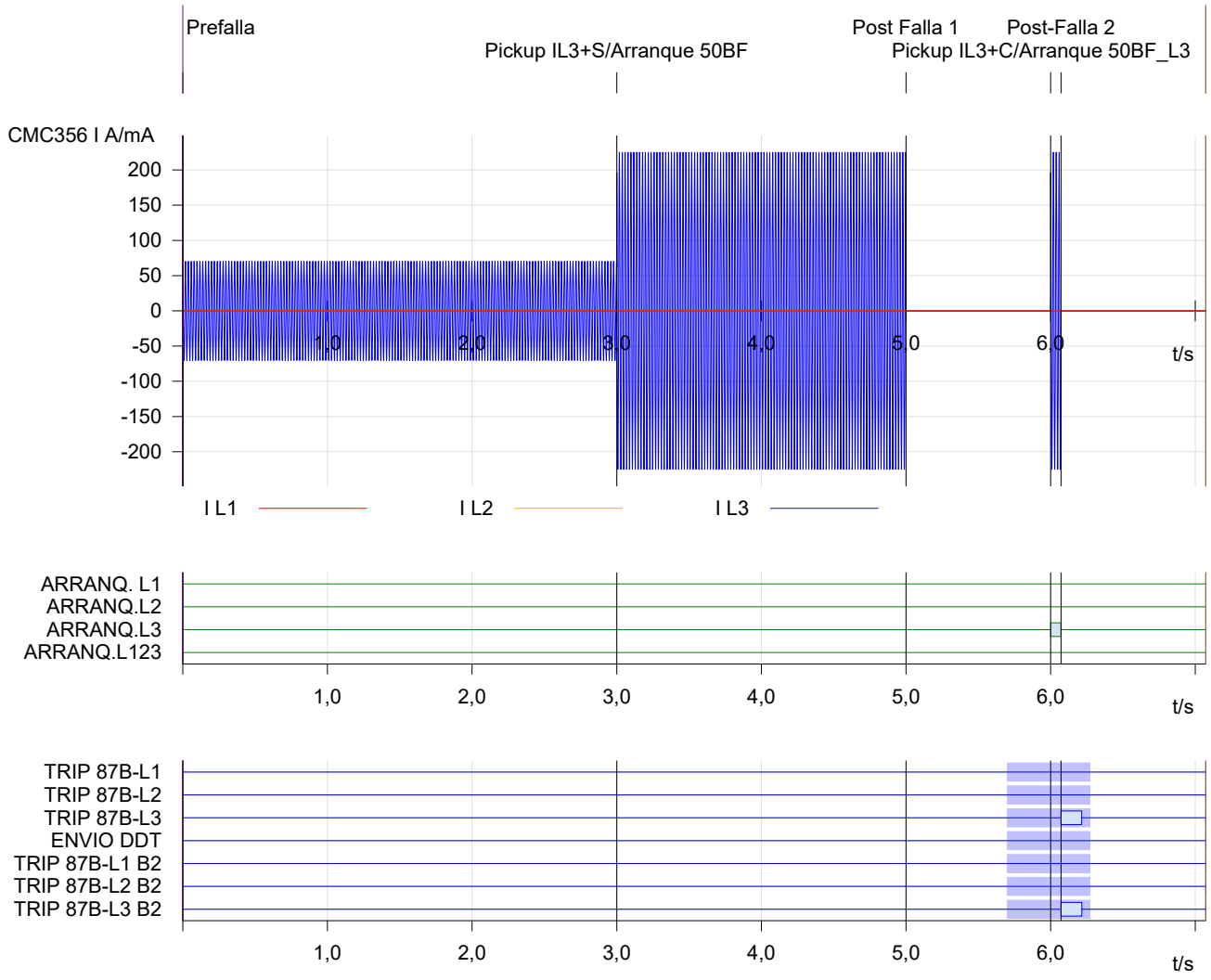
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL3+C/Arranque 50BF_L3	Pickup IL3+C/Arranque 50BF_L3	TRIP 87B-L3 0>1	50,00 ms	30,00 ms	30,00 ms	71,60 ms	21,60 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL3+S/Arranque 50BF	Post Falla 1	Pickup IL3+C/Arranque 50BF_L3	Post-Falla 2
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	0	0
TRIP 87B-L2	0	0	0	0	0
TRIP 87B-L3	0	0	0	1	0
ENVIO DDT	0	0	0	0	0
TRIP 87B-L1 B2	0	0	0	0	0
TRIP 87B-L2 B2	0	0	0	0	0
TRIP 87B-L3 B2	0	0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,072 s	<none>	n/a
C2 - C1	7,072 s		n/a

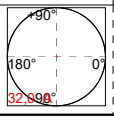
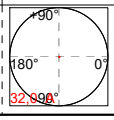
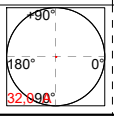
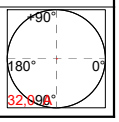
Event recorder

Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ.L3	0>1
6,071 s	Input	TRIP 87B-L3 B2	0>1
6,072 s	Input	TRIP 87B-L3	0>1
6,072 s	Output	ARRANQ.L3	1>0
6,214 s	Input	TRIP 87B-L3	1>0
6,216 s	Input	TRIP 87B-L3 B2	1>0

Test State:
Test passed

9.4 Operacion 50BF_Fase L123:

Test Settings

State	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L123	Post-Falla 3
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	0	0
ARRANQ.L2	0	0	0	0	0
ARRANQ.L3	0	0	0	0	0
ARRANQ.L123	0	0	0	1	0
Max. State Time	3,000 s	2,000 s	1,000 s	100,0 ms	1,000 s
Trigger Logic				AND	
TRIP 87B-L1				1	
TRIP 87B-L2				1	
TRIP 87B-L3				1	
TRIP 87B-L1 B2				1	
TRIP 87B-L2 B2				1	
TRIP 87B-L3 B2				1	
User interaction	no	no	no	no	no
CMGPS trigger	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no
Pulses / seconds	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no
Diagrams					

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:05:32	Test End:	11-abr.-2019 03:05:41
User Name:		Manager:	
Company:			

Test Results

Time Assessment

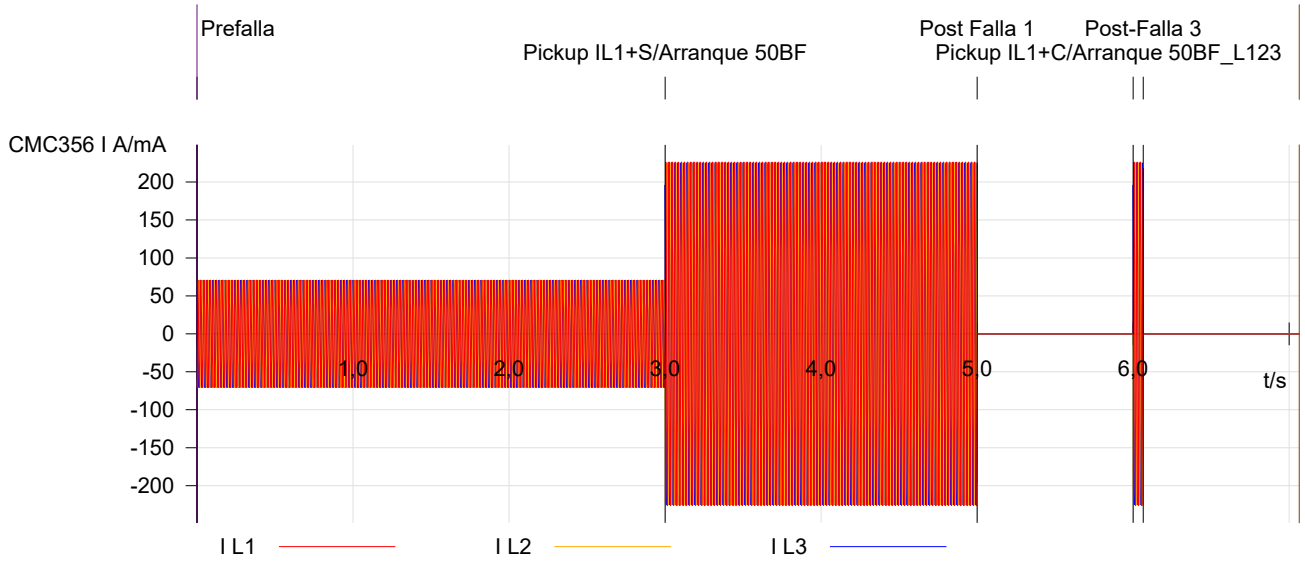
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL1+C/Arranque 50BF_L123	Pickup IL1+C/Arranque 50BF_L123	TRIP 87B-L3 0>1	50,00 ms	20,00 ms	20,00 ms	63,90 ms	13,90 ms	+

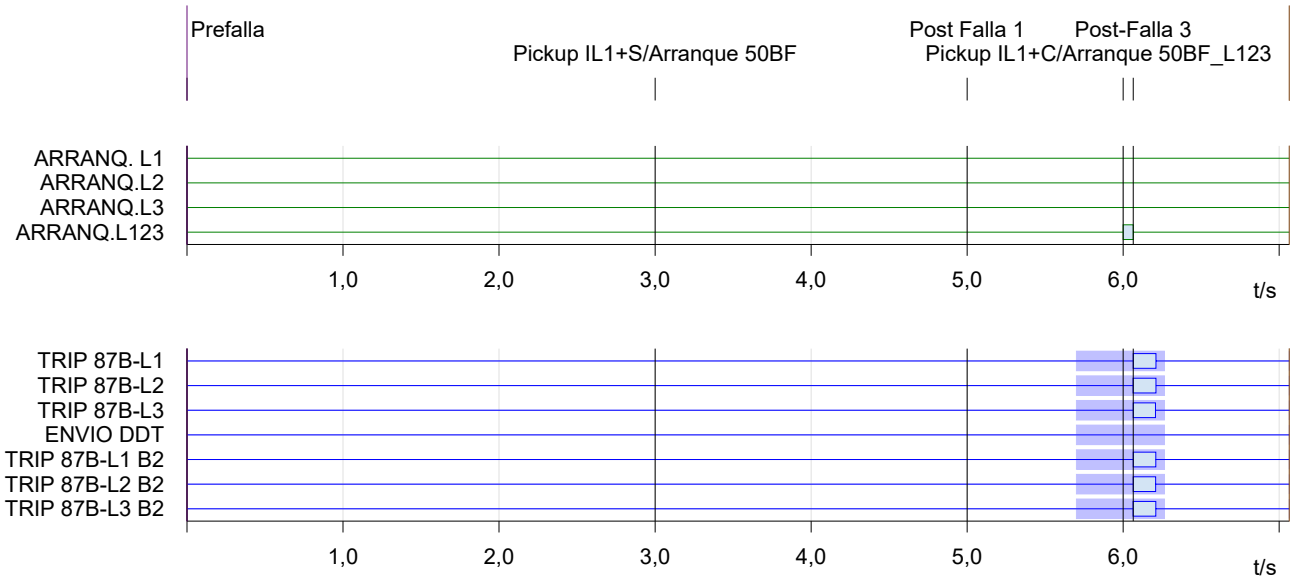
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L123	Post-Falla 3
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	1	0
TRIP 87B-L2	0	0	0	1	0
TRIP 87B-L3	0	0	0	1	0
ENVIO DDT	0	0	0	0	0
TRIP 87B-L1 B2	0	0	0	1	0
TRIP 87B-L2 B2	0	0	0	1	0
TRIP 87B-L3 B2	0	0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

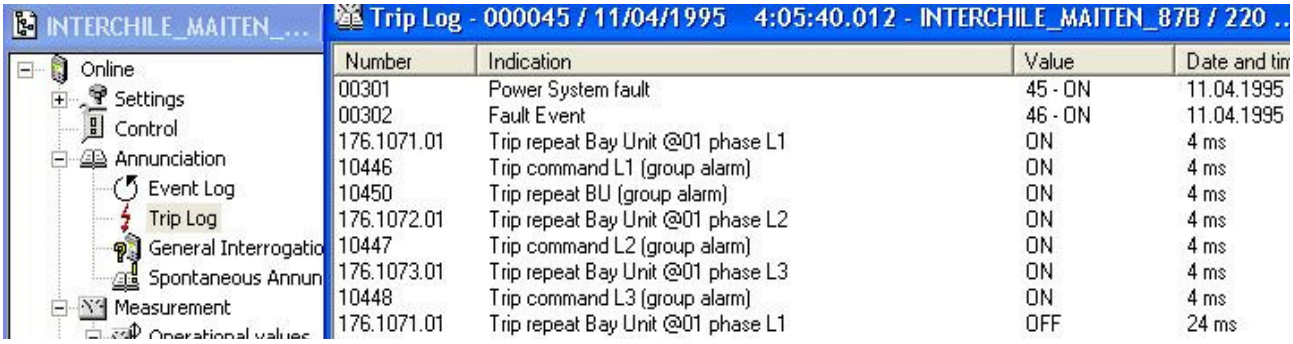
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,064 s	<none>	n/a
C2 - C1	7,064 s		n/a

Event recorder

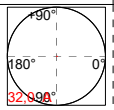
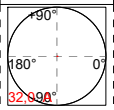
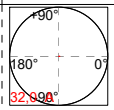
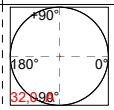
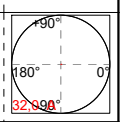
Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ.L123	0>1
6,064 s	Input	TRIP 87B-L3 B2	0>1
6,064 s	Input	TRIP 87B-L2	0>1
6,064 s	Input	TRIP 87B-L3	0>1
6,064 s	Input	TRIP 87B-L1 B2	0>1
6,064 s	Input	TRIP 87B-L2 B2	0>1
6,064 s	Input	TRIP 87B-L1	0>1
6,064 s	Output	ARRANQ.L123	1>0
6,207 s	Input	TRIP 87B-L3	1>0
6,208 s	Input	TRIP 87B-L2 B2	1>0
6,209 s	Input	TRIP 87B-L3 B2	1>0
6,209 s	Input	TRIP 87B-L1 B2	1>0
6,210 s	Input	TRIP 87B-L2	1>0
6,210 s	Input	TRIP 87B-L1	1>0

Test State:

Test passed



Test Settings

State	Prefalla	Pickup IL1+S/Arranque 50BF_L1	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	Post-Falla 2
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	1	1	0
ARRANQ.L2	0	0	0	0	0	0
ARRANQ.L3	0	0	0	0	0	0
ARRANQ.L123	0	0	0	0	0	0
Max. State Time	3,000 s	2,000 s	1,000 s			1,000 s
Trigger Logic				AND	AND	
TRIP 87B-L1				1	X	
ENVIO DDT				X	1	
TRIP 87B-L1 B2				1	X	
User interaction	no	no	no	no	no	no
CMGPS trigger	no	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no	no
Pulses / seconds	1	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no	no
Diagrams						

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:08:40	Test End:	11-abr.-2019 03:08:48
User Name:		Manager:	
Company:			

Test Results

Time Assessment

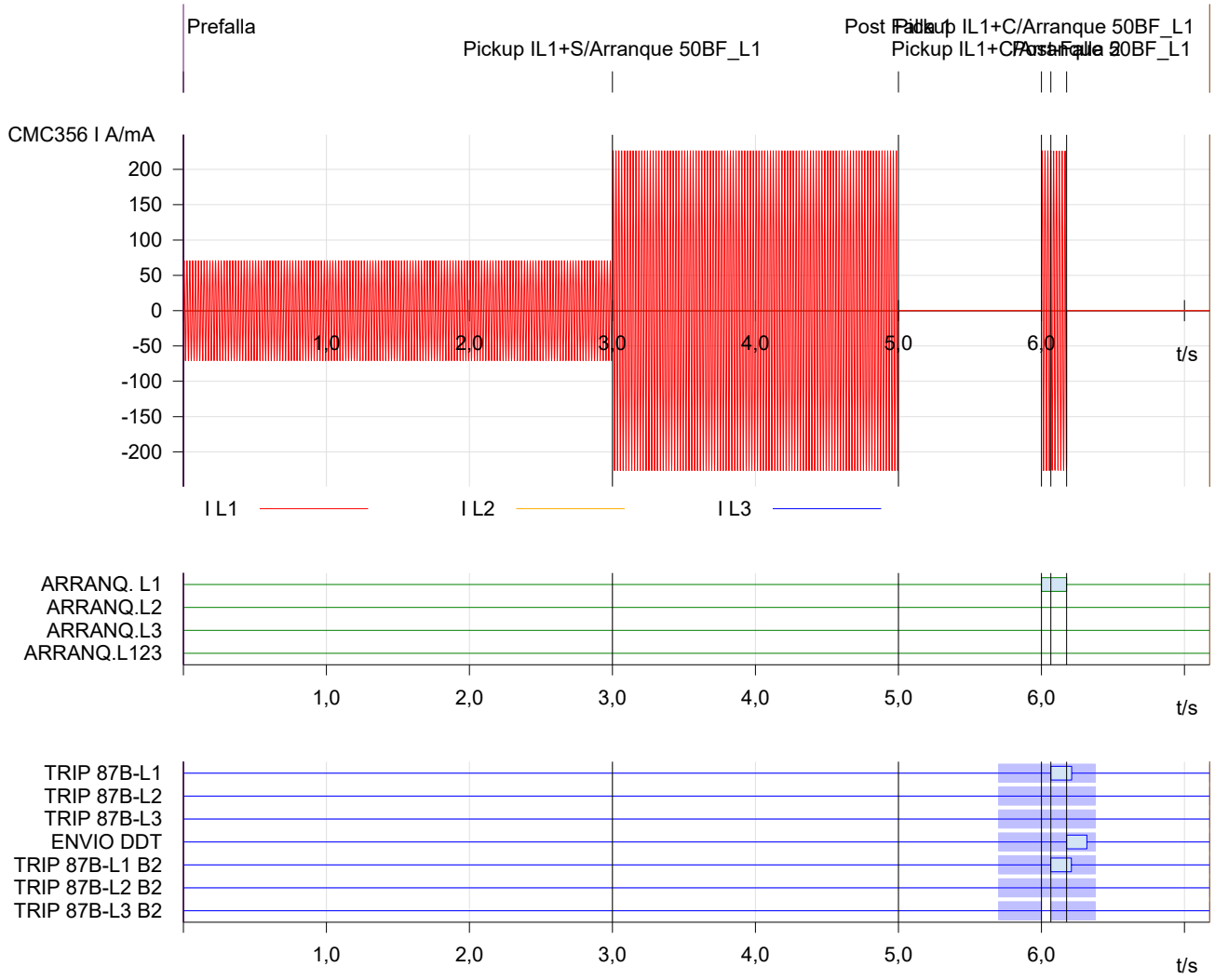
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	TRIP 87B-L1 0>1	50,00 ms	30,00 ms	30,00 ms	65,20 ms	15,20 ms	+
Disp. 50BF_Etapa 2	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	ENVIO DDT 0>1	150,0 ms	30,00 ms	30,00 ms	176,1 ms	26,10 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL1+S/Arranque 50BF_L1	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	Post-Falla 2
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	500,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	1	1	0
TRIP 87B-L2	0	0	0	0	0	0
TRIP 87B-L3	0	0	0	0	0	0
ENVIO DDT	0	0	0	0	1	0
TRIP 87B-L1 B2	0	0	0	1	1	0
TRIP 87B-L2 B2	0	0	0	0	0	0
TRIP 87B-L3 B2	0	0	0	X	0	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

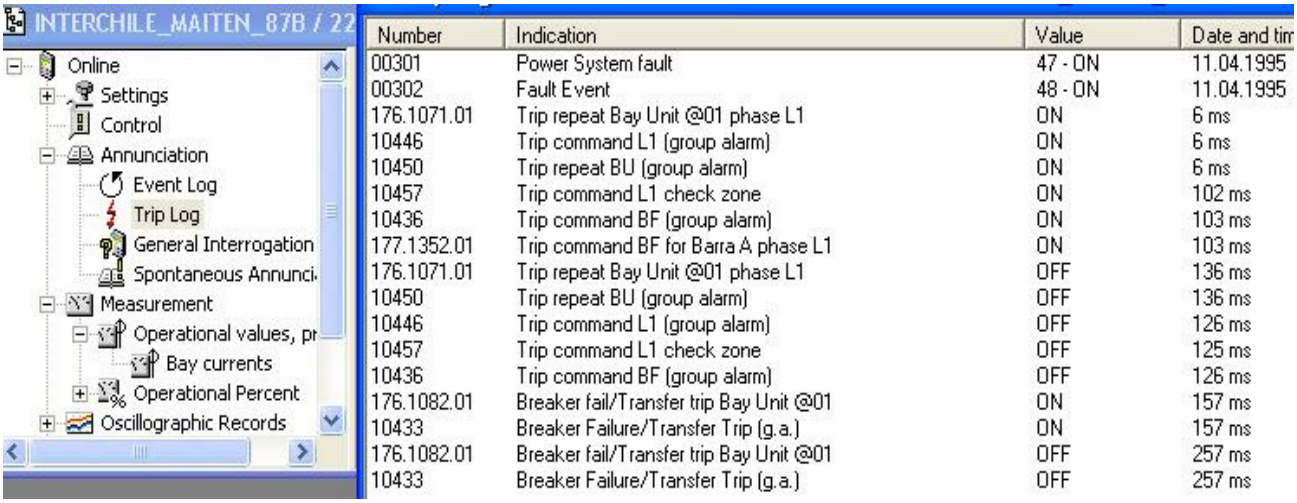
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,176 s	<none>	n/a
C2 - C1	7,176 s		n/a

Event recorder

Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ. L1	0>1
6,065 s	Input	TRIP 87B-L1 B2	0>1
6,065 s	Input	TRIP 87B-L1	0>1
6,176 s	Input	ENVIO DDT	0>1
6,176 s	Output	ARRANQ. L1	1>0
6,210 s	Input	TRIP 87B-L1 B2	1>0
6,212 s	Input	TRIP 87B-L1	1>0
6,317 s	Input	ENVIO DDT	1>0

Test State:

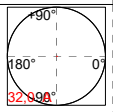
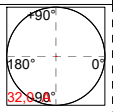
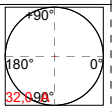
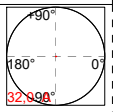
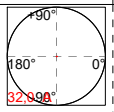
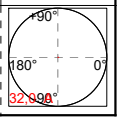
Test passed



10.2 Operacion 50BF_Fase L2:

Test Settings

State	Prefalla	Pickup IL2+S/Arranque 50BF_L2	Post Falla 1	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	Post-Falla 2
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	300,0 mA -120,00 ° 50,000 Hz	300,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

ARRANQ. L1	0	0	0	0	0	0
ARRANQ.L2	0	0	0	1	1	0
ARRANQ.L3	0	0	0	0	0	0
ARRANQ.L123	0	0	0	0	0	0
Max. State Time	3,000 s	2,000 s	1,000 s			1,000 s
Trigger Logic				AND	AND	
TRIP 87B-L2				1	X	
ENVIO DDT				X	1	
TRIP 87B-L2 B2				1	X	
User interaction	no	no	no	no	no	no
CMGPS trigger	no	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no	no
Pulses / seconds	1	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no	no
Diagrams						

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:13:07	Test End:	11-abr.-2019 03:13:16
User Name:		Manager:	
Company:			

Test Results

Time Assessment

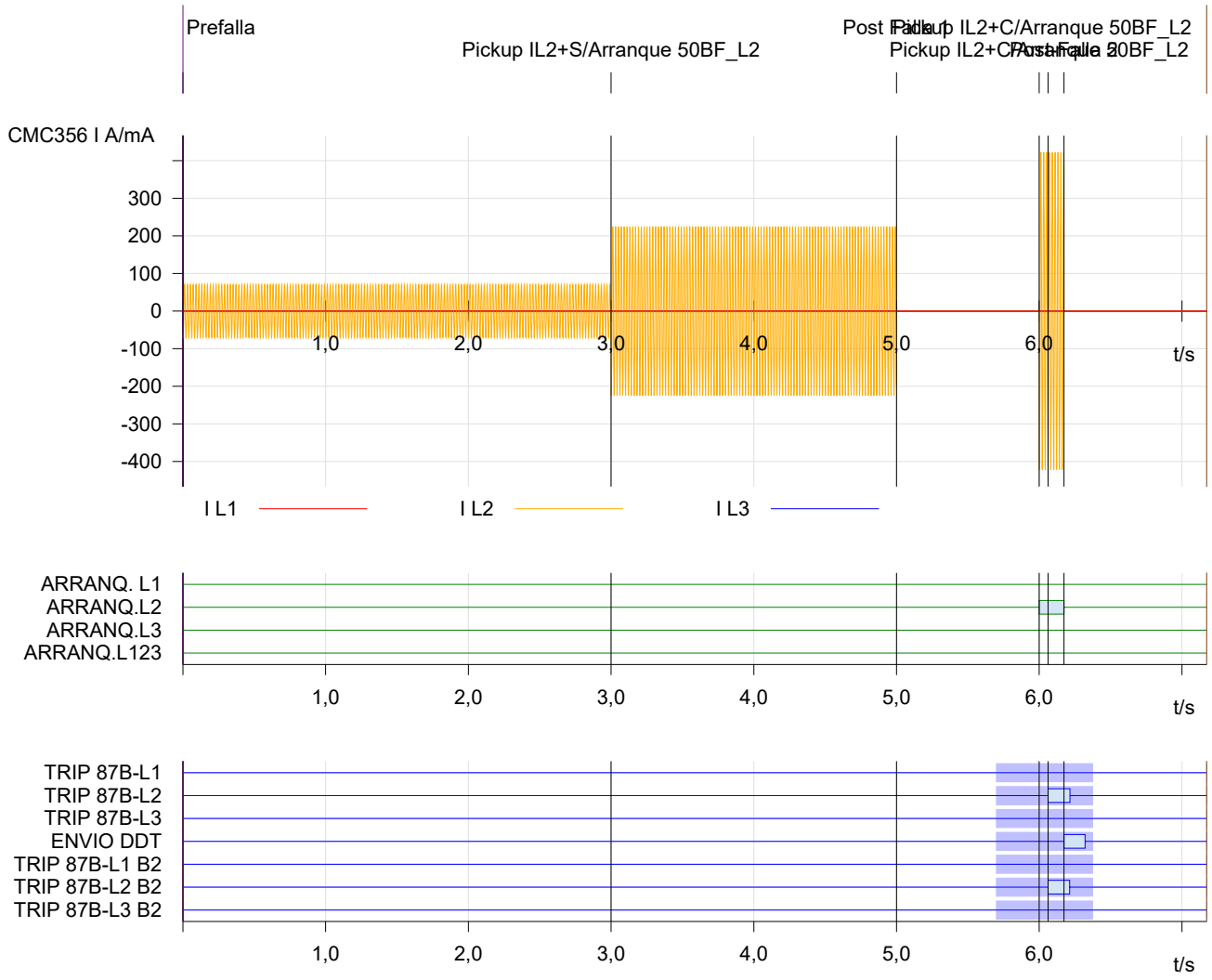
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	TRIP 87B-L2 0>1	50,00 ms	30,00 ms	30,00 ms	62,10 ms	12,10 ms	+
Disp. 50BF_Etapa 2	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	ENVIO DDT 0>1	150,0 ms	30,00 ms	30,00 ms	173,2 ms	23,20 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL2+S/Arranque 50BF_L2	Post Falla 1	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	Post-Falla 2
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	300,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	0	0	0
TRIP 87B-L2	0	0	0	1	0	0
TRIP 87B-L3	0	0	0	0	0	0
ENVIO DDT	0	0	0	0	1	0
TRIP 87B-L1 B2	0	0	0	0	0	0
TRIP 87B-L2 B2	0	0	0	1	0	0
TRIP 87B-L3 B2	0	0	0	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

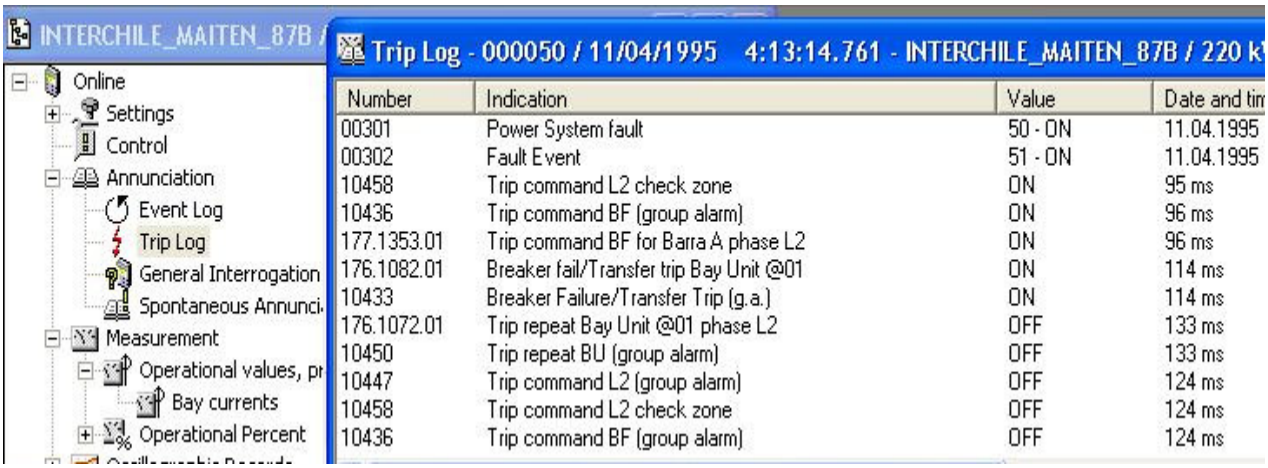
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,173 s	<none>	n/a
C2 - C1	7,173 s		n/a

Event recorder

Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ.L2	0>1
6,062 s	Input	TRIP 87B-L2	0>1
6,062 s	Input	TRIP 87B-L2 B2	0>1
6,173 s	Input	ENVIO DDT	0>1
6,173 s	Output	ARRANQ.L2	1>0
6,214 s	Input	TRIP 87B-L2 B2	1>0
6,216 s	Input	TRIP 87B-L2	1>0
6,322 s	Input	ENVIO DDT	1>0

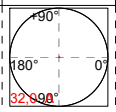
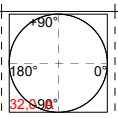
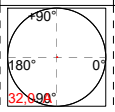
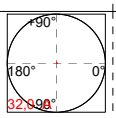
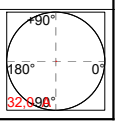
Test State:

Test passed



10.3 Operacion 50BF_Fase L3:

Test Settings

State	Prefalla	Pickup IL3+S/Arranque 50BF_L3	Post Falla 1	Pickup IL3+C/Arranque 50BF_L3	Pickup IL3+C/Arranque 50BF_L3	Post-Falla 3
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	300,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	0	0	0
ARRANQ.L2	0	0	0	0	0	0
ARRANQ.L3	0	0	0	1	1	0
ARRANQ.L123	0	0	0	0	0	0
Max. State Time	3,000 s	2,000 s	1,000 s			1,000 s
Trigger Logic				AND	AND	
TRIP 87B-L3				1	X	
ENVIO DDT				X	1	
TRIP 87B-L3 B2				1	X	
User interaction	no	no	no	no	no	no
CMGPS trigger	no	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no	no
Pulses / seconds	1	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no	no
Diagrams						

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:16:22	Test End:	11-abr.-2019 03:16:31
User Name:		Manager:	
Company:			

Test Results

Time Assessment

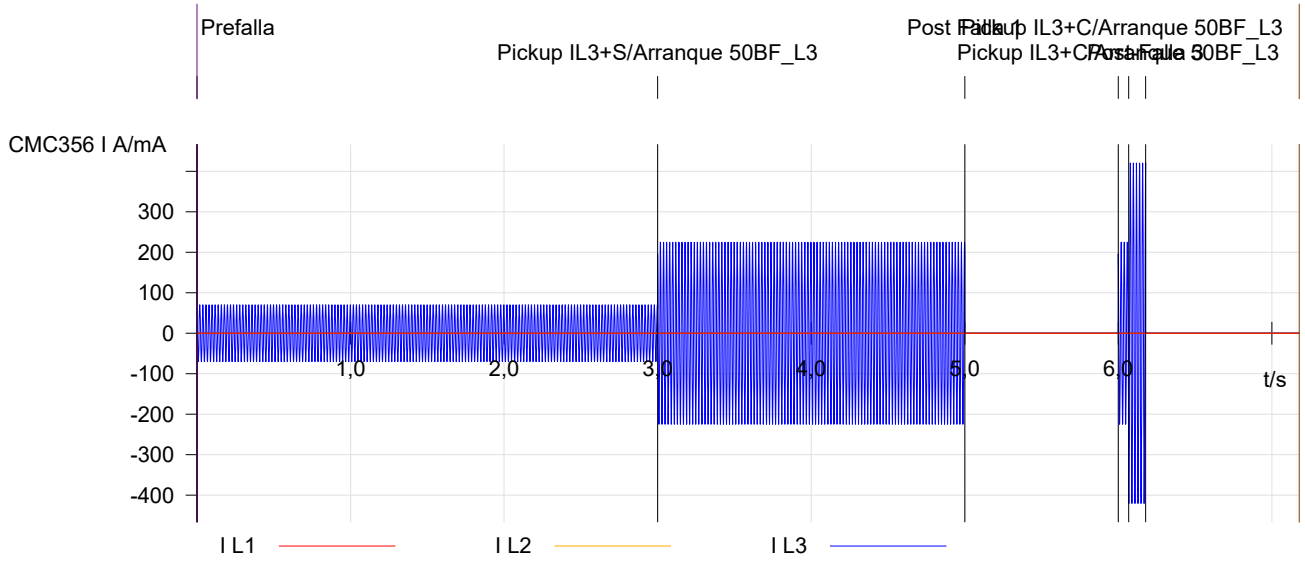
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL3+C/Arranque 50BF_L3	Pickup IL3+C/Arranque 50BF_L3	TRIP 87B-L3 0>1	50,00 ms	30,00 ms	30,00 ms	66,90 ms	16,90 ms	+
Disp. 50BF_Etapa 2	Pickup IL3+C/Arranque 50BF_L3	Pickup IL3+C/Arranque 50BF_L3	ENVIO DDT 0>1	150,0 ms	30,00 ms	30,00 ms	178,1 ms	28,10 ms	+

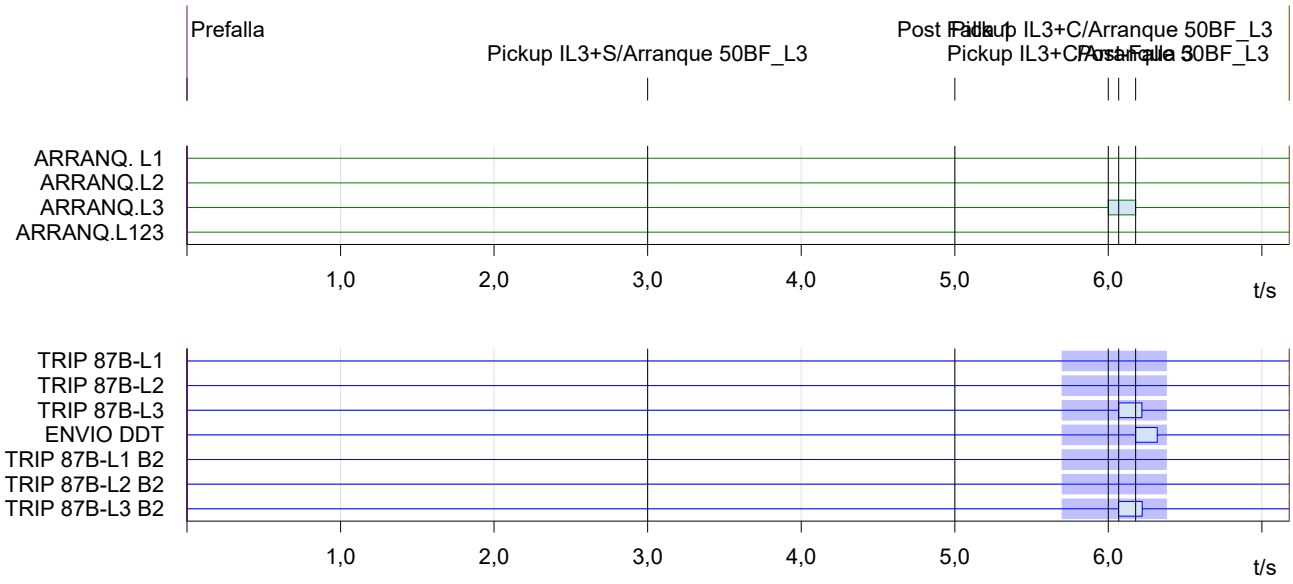
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL3+S/Arranque 50BF_L3	Post Falla 1	Pickup IL3+C/Arranque 50BF_L3	Pickup IL3+C/Arranque 50BF_L3	Post-Falla 3
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	300,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	0	0	0
TRIP 87B-L2	0	0	0	0	0	0
TRIP 87B-L3	0	0	0	1	0	0
ENVIO DDT	0	0	0	0	1	0
TRIP 87B-L1 B2	0	0	0	0	0	0
TRIP 87B-L2 B2	0	0	0	0	0	0
TRIP 87B-L3 B2	0	0	0	1	0	0

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

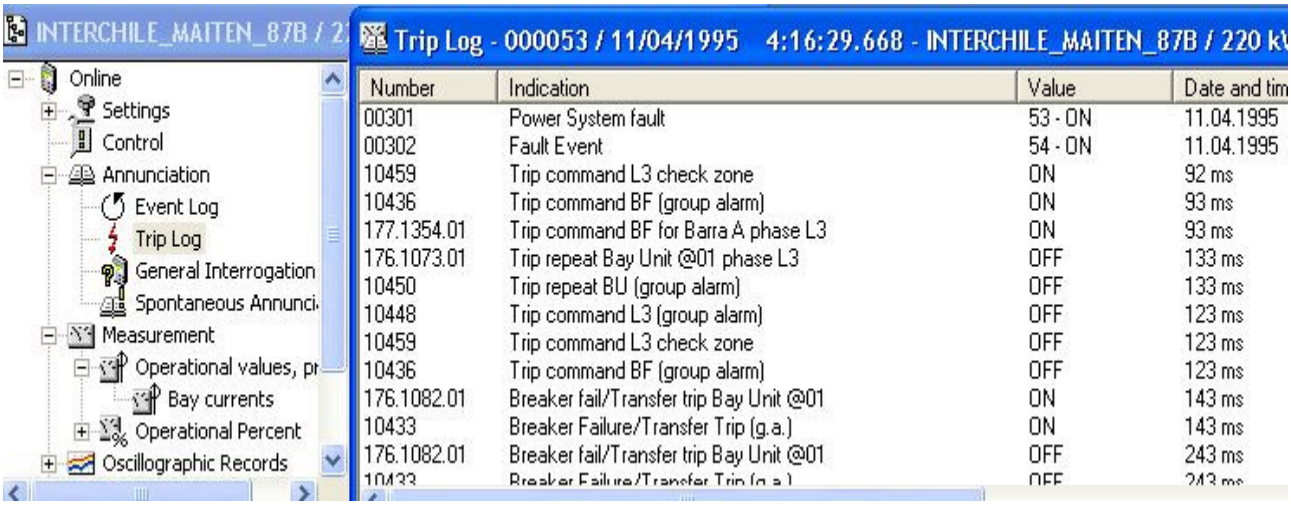
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,178 s	<none>	n/a
C2 - C1	7,178 s		n/a

Event recorder

Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ.L3	0>1
6,067 s	Input	TRIP 87B-L3 B2	0>1
6,067 s	Input	TRIP 87B-L3	0>1
6,178 s	Input	ENVIO DDT	0>1
6,178 s	Output	ARRANQ.L3	1>0
6,219 s	Input	TRIP 87B-L3	1>0
6,221 s	Input	TRIP 87B-L3 B2	1>0
6,318 s	Input	ENVIO DDT	1>0

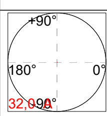
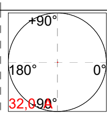
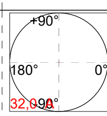
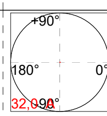
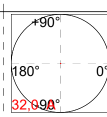
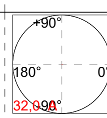
Test State:

Test passed



10.4 Operacion 50BF_Fase L123:

Test Settings

State	Prefalla	Pickup IL2+S/Arranque 50BF_L123	Post Falla 1	Pickup IL2+C/Arranque 50BF_L123	Pickup IL1+C/Arranque 50BF_L123	Post-Falla 3
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	0	0	0
ARRANQ.L2	0	0	0	0	0	0
ARRANQ.L3	0	0	0	0	0	0
ARRANQ.L123	0	0	0	1	1	0
Max. State Time	3,000 s	2,000 s	1,000 s			1,000 s
Trigger Logic				AND	AND	
TRIP 87B-L1				1	X	
TRIP 87B-L2				1	X	
TRIP 87B-L3				1	X	
ENVIO DDT				X	1	
TRIP 87B-L1 B2				1	1	
TRIP 87B-L2 B2				1	X	
TRIP 87B-L3 B2				1	X	
User interaction	no	no	no	no	no	no
CMGPS trigger	no	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no	no
Pulses / seconds	1	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no	no
Diagrams						

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:19:34	Test End:	11-abr.-2019 03:19:43
User Name:		Manager:	
Company:			

Test Results

Time Assessment

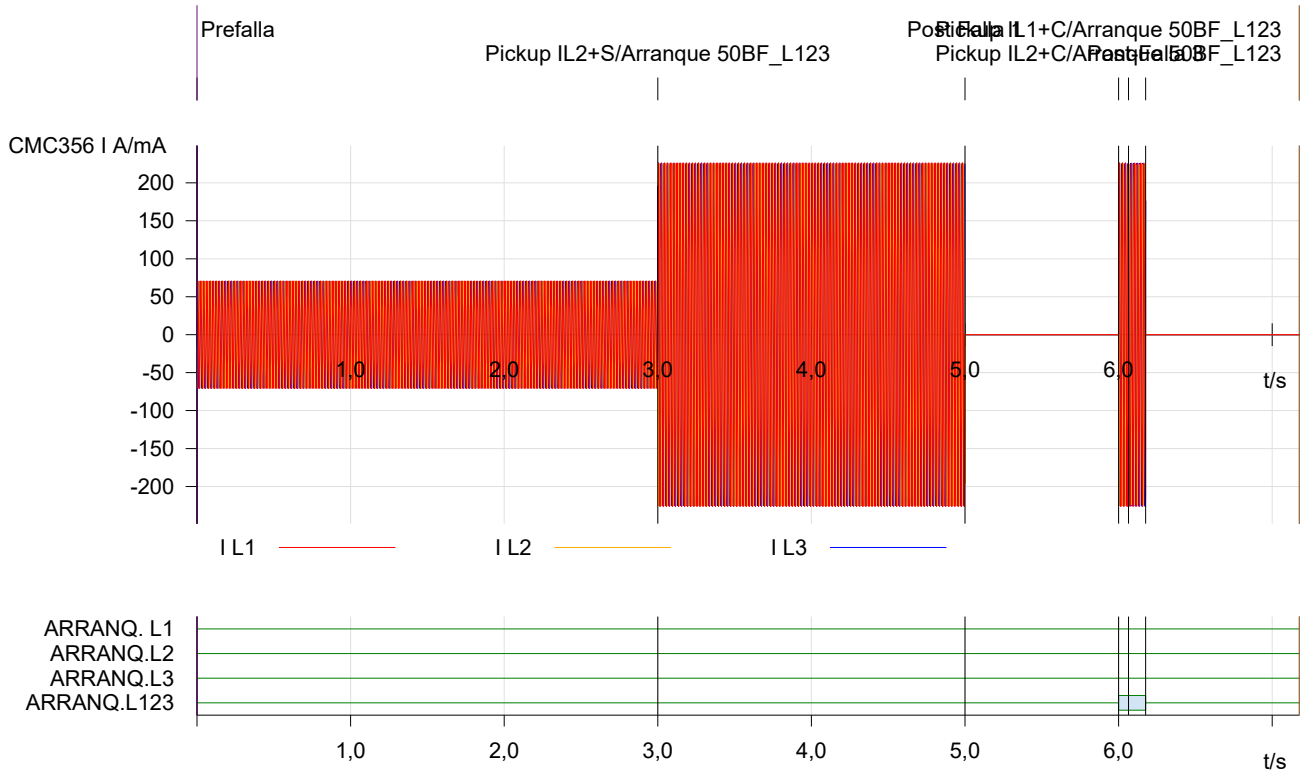
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL2+C/Arranque 50BF_L123	Pickup IL2+C/Arranque 50BF_L123	TRIP 87B-L3 B2 0>1	50,00 ms	30,00 ms	30,00 ms	64,60 ms	14,60 ms	+
Disp. 50BF_Etapa 2	Pickup IL2+C/Arranque 50BF_L123	Pickup IL2+C/Arranque 50BF_L123	ENVIO DDT 0>1	150,0 ms	30,00 ms	30,00 ms	176,2 ms	26,20 ms	+

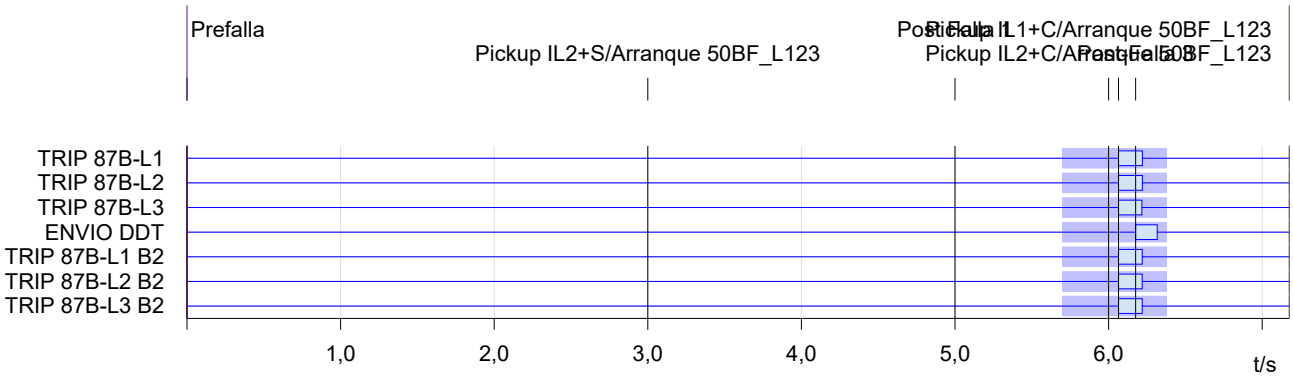
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL2+S/Arranque 50BF_L123	Post Falla 1	Pickup IL2+C/Arranque 50BF_L123	Pickup IL1+C/Arranque 50BF_L123	Post-Falla 3
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	300,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	1	0	0
TRIP 87B-L2	0	0	0	1	0	0
TRIP 87B-L3	0	0	0	1	0	0
ENVIO DDT	0	0	0	0	1	0
TRIP 87B-L1 B2	0	0	0	1	0	0
TRIP 87B-L2 B2	0	0	0	1	0	0
TRIP 87B-L3 B2	0	0	0	1	0	0

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

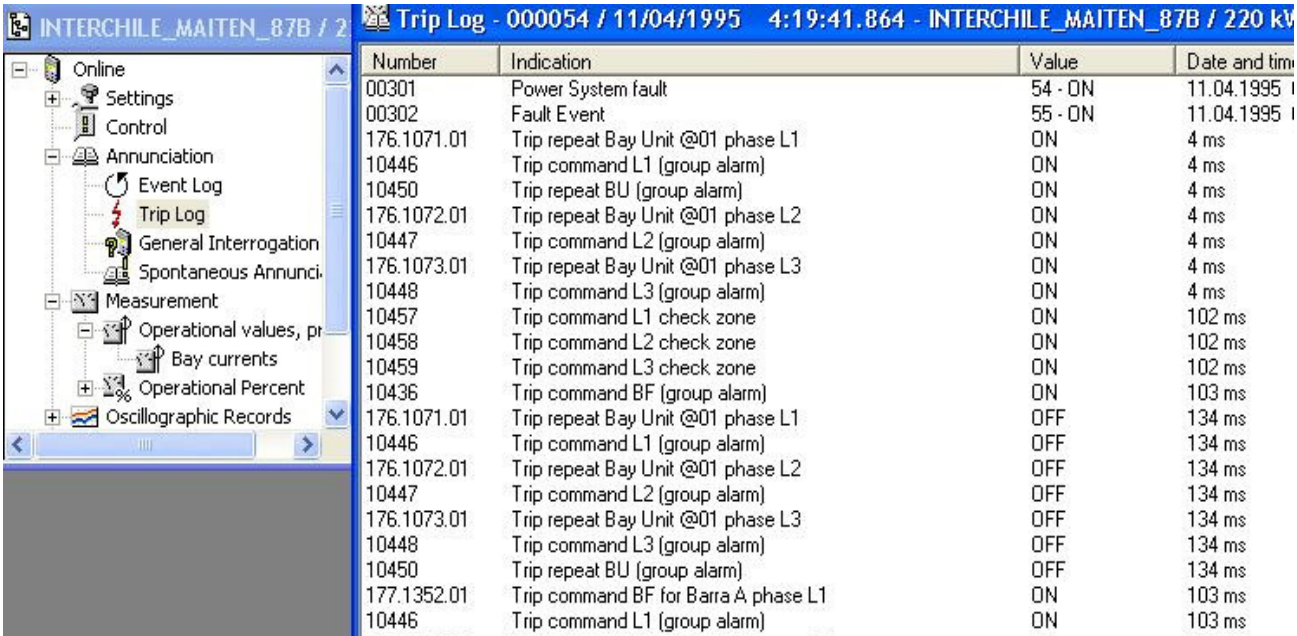
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,176 s	<none>	n/a
C2 - C1	7,176 s		n/a

Event recorder

Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ.L123	0>1
6,065 s	Input	TRIP 87B-L3 B2	0>1
6,065 s	Input	TRIP 87B-L2	0>1
6,065 s	Input	TRIP 87B-L1 B2	0>1
6,065 s	Input	TRIP 87B-L3	0>1
6,065 s	Input	TRIP 87B-L1	0>1
6,065 s	Input	TRIP 87B-L2 B2	0>1
6,176 s	Input	ENVIO DDT	0>1
6,176 s	Output	ARRANQ.L123	1>0
6,217 s	Input	TRIP 87B-L3	1>0
6,218 s	Input	TRIP 87B-L2 B2	1>0
6,219 s	Input	TRIP 87B-L3 B2	1>0
6,219 s	Input	TRIP 87B-L1 B2	1>0
6,220 s	Input	TRIP 87B-L1	1>0
6,220 s	Input	TRIP 87B-L2	1>0
6,316 s	Input	ENVIO DDT	1>0

Test State:

Test passed



Group end:11. Operacion 50BF_J2 (T1 and T2)

Group:12. Operacion End Fault_50BF E0

Hardware

Test Equipment

Type	Serial Number
CMC356	MC355V

Hardware Check

Performed At	Result	Details
11-04-2019 3:22:55	Passed	

Analog Outputs

Test Equipment		Test Object		
Device	**Connector**	**Display Name**	**Connection Terminal**	
CMC356 I A MC355V	1 2 3 N	I L1 I L2 I L3		

Binary/Analog Inputs

Test Equipment		Test Object		
Device	**Connector**	**Display Name**	**Connection Terminal**	
CMC356 MC355V	1+ 1- 2+ 2- 3+ 3- 4+ 4- 5+ 5- 6+ 6- 7+ 7- 8+ 8- 9+ 9- 10+ 10- 1 2 N	Disp.L1_52J2 Disp.L2_52J2 Disp.L3_52J2 DDT Etapa 0 50BF ET0 Bin. in 6 Bin. in 7 Bin. in 8 Bin. in 9 Bin. in 10 Bin. in 11 Bin. in 12		

Binary Outputs

Test Equipment		Test Object		
Device	**Connector**	**Display Name**	**Connection Terminal**	
CMC356 MC355V	1+ 1- 2+ 2- 3+ 3- 4+ 4- 11 12 13 14 N	52J2_Open 52J2_Close Bin. out 3 Bin. out 4 Bin. out 5 Bin. out 6 Bin. out 7 Bin. out 8		

Analog DC Inputs

Test Equipment		Test Object		
Device	**Connector**	**Display Name**	**Connection Terminal**	

Group:12.1 Verificacion Pickup_End Fault

12.1.1 Pickup con Arranque Fase L1:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J2_Open	1
52J2_Close	0

dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52J2	X
Disp.L2_52J2	X
Disp.L3_52J2	X
DDT Etapa 0	1
50BF ET0	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 03:37:19	Test End:	11-abr.-2019 03:37:26
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	DDT Etapa 0 0->1 and 50BF ET0 0->1	I L1	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	45,40 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

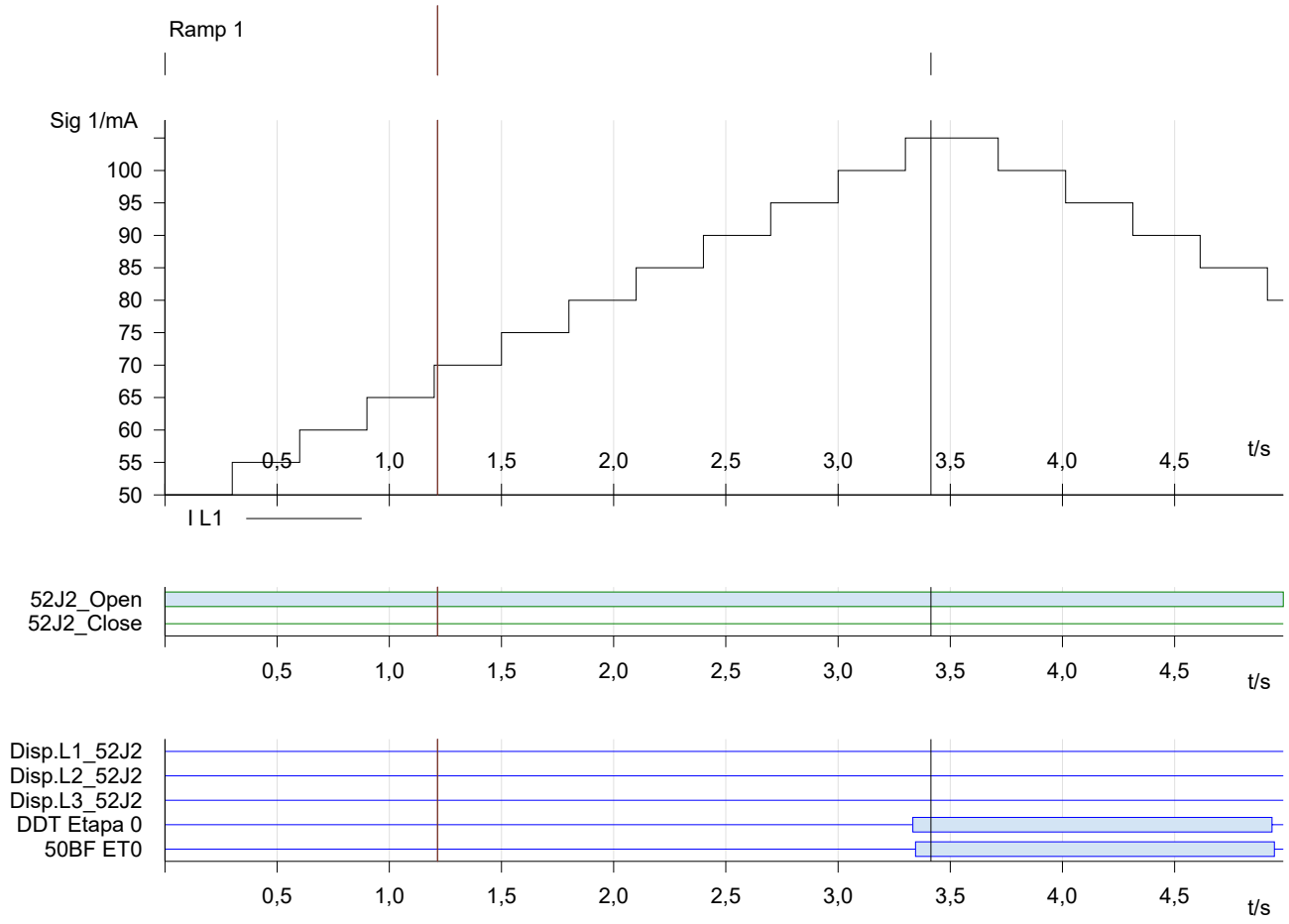
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:

Test passed

12.1.2 Pickup con Arranque Fase L2:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J2_Open	1
52J2_Close	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52J2	X
Disp.L2_52J2	X
Disp.L3_52J2	X
DDT Etapa 0	1
50BF ET0	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 03:37:35	Test End:	11-abr.-2019 03:37:43
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	50BF ET0 0->1 and DDT Etapa 0 0->1	I L2	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	40,80 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

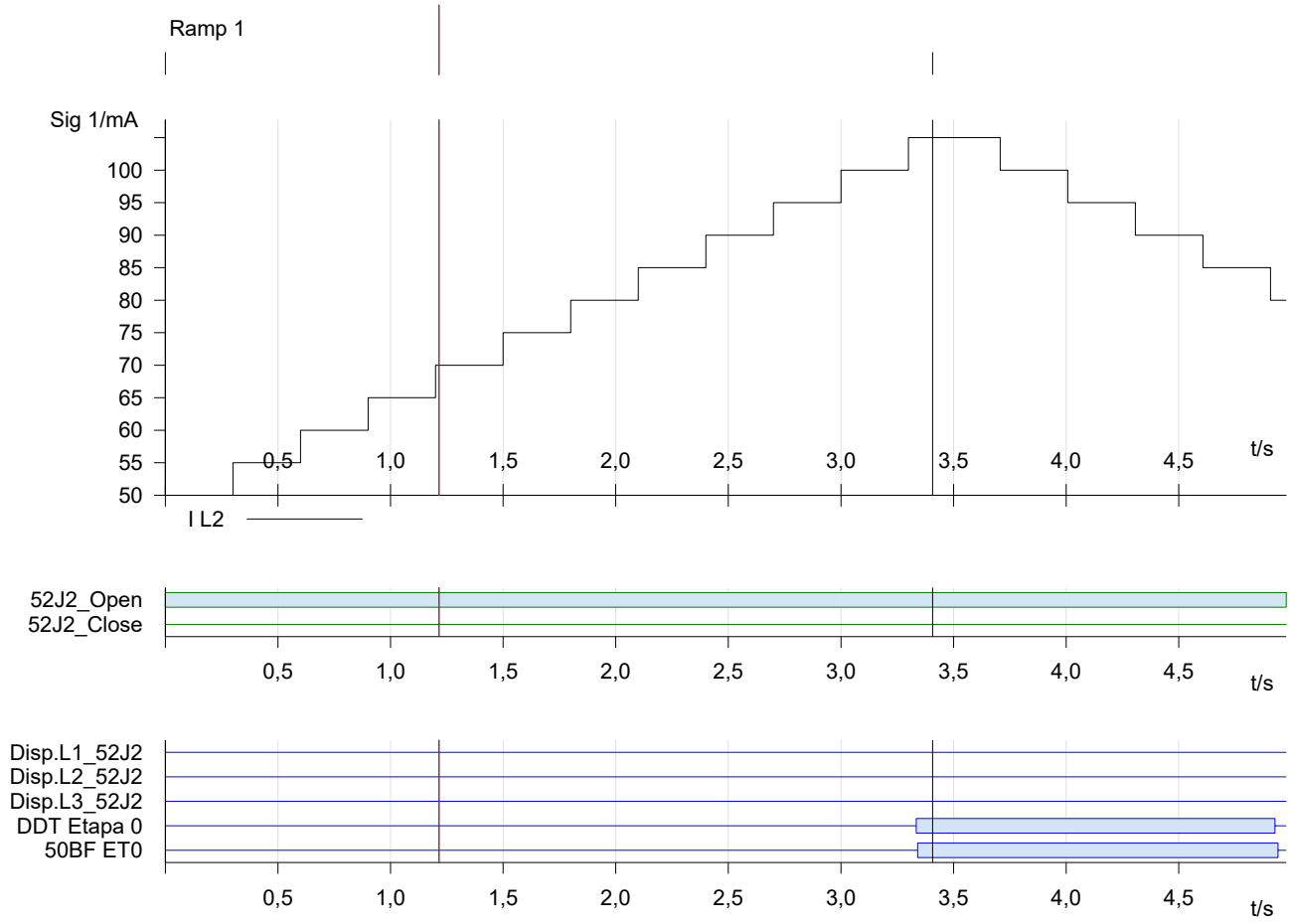
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:

Test passed

12.1.3 Pickup con Arranque Fase L3:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J2_Open	1
52J2_Close	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52J2	X
Disp.L2_52J2	X
Disp.L3_52J2	X
DDT Etapa 0	1
50BF ET0	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 03:37:50
Test End: 11-abr.-2019 03:37:56
User Name:
Manager:
Company:

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	50BF ET0 0->1 and DDT Etapa 0 0->1	I L3	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	40,20 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

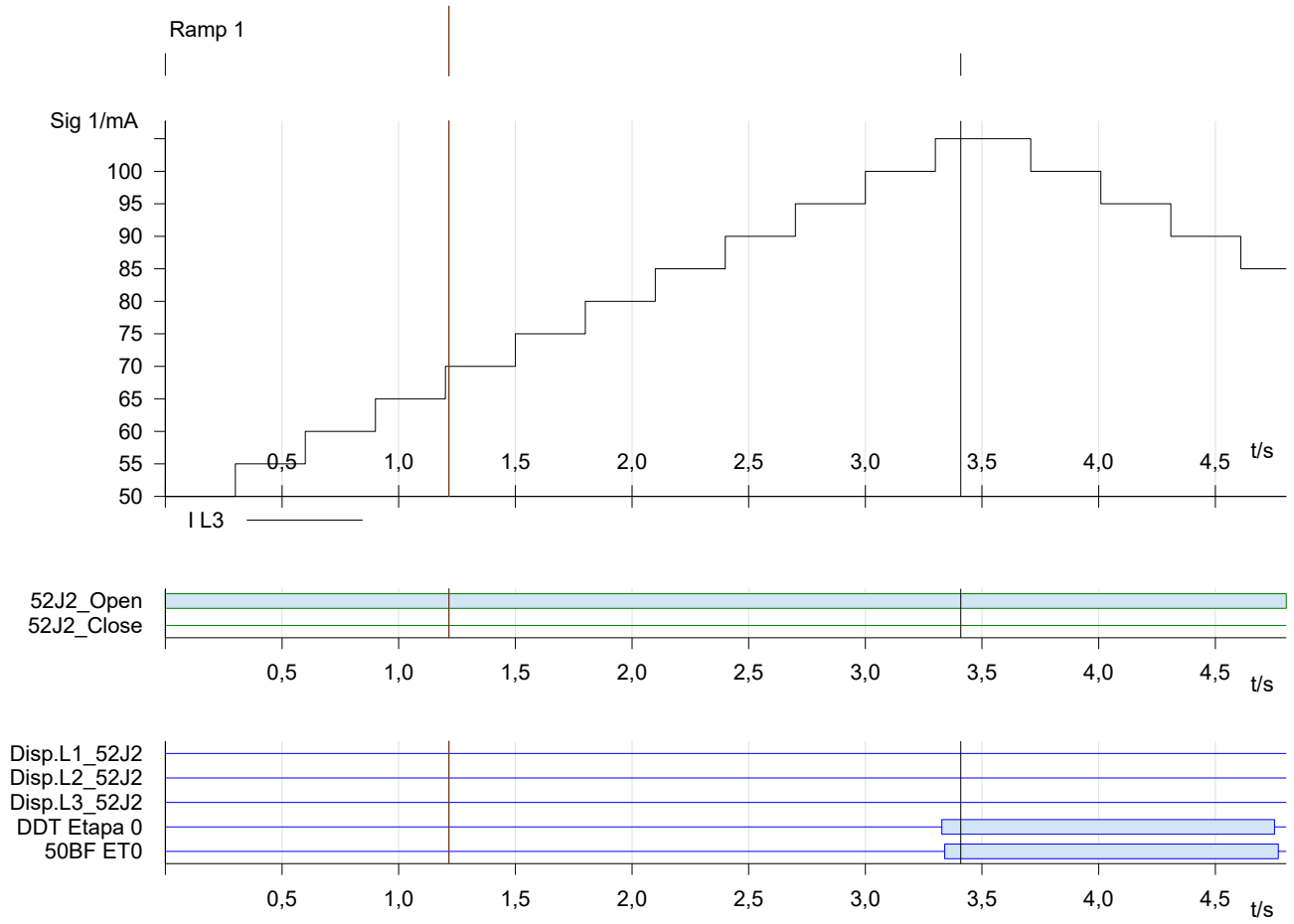
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:

Test passed

12.1.4 Pickup con Arranque Fase L123:

Test Settings

General

No. of ramp states:	1
Total steps per test:	23
Total time per test:	6,900 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J2_Open	1
52J2_Close	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52J2	X
Disp.L2_52J2	X
Disp.L3_52J2	X
DDT Etapa 0	1
50BF ET0	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 03:38:09	Test End:	11-abr.-2019 03:38:16
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	50BF ET0 0->1 and DDT Etapa 0 0->1	I L1; L2; L3	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	35,80 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

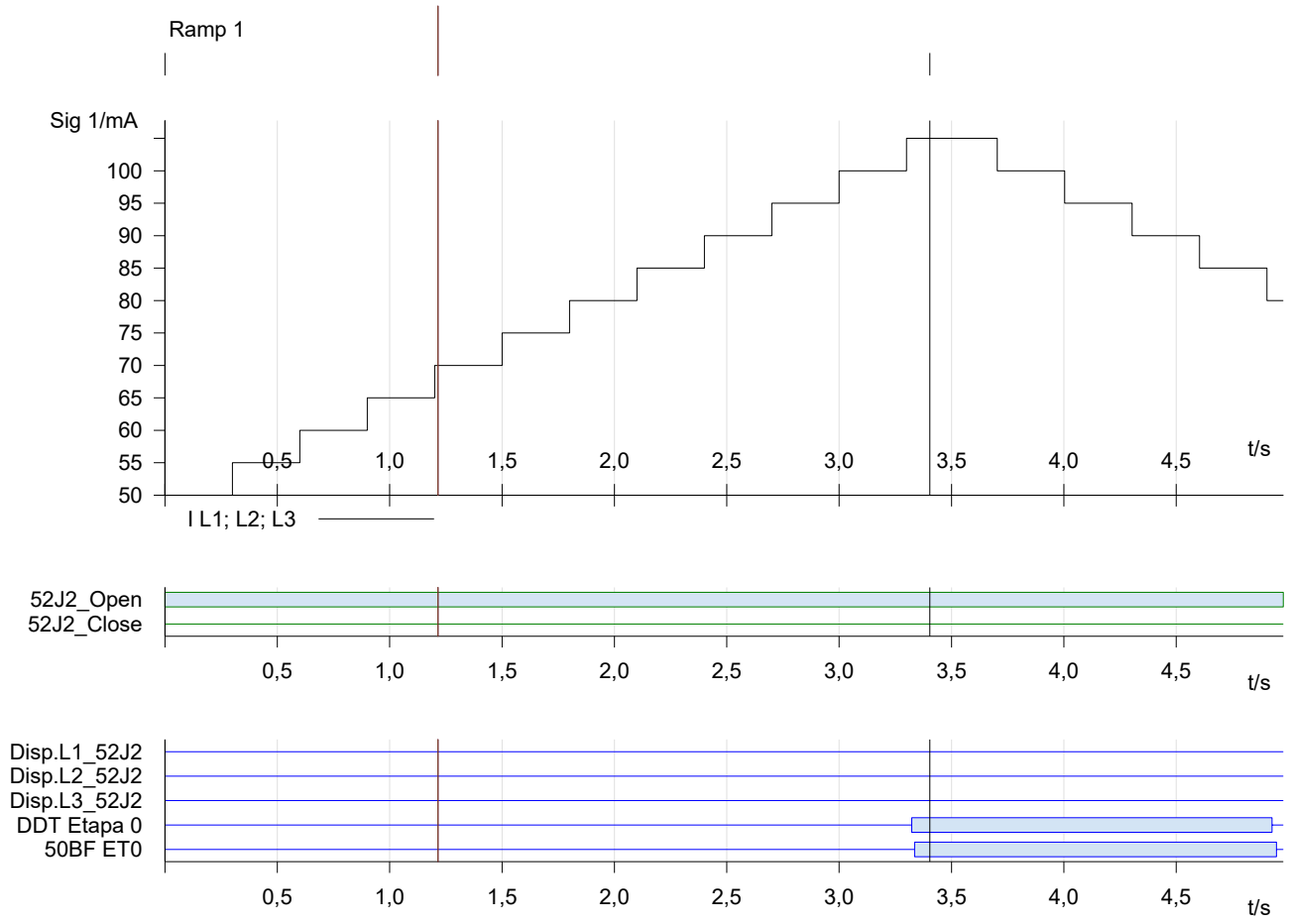
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	1,215 s	<none>	n/a

Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:
Test passed

12.1.4 Pickup CB Close Fase L123:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J2_Open	0
52J2_Close	1
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52J2	X
Disp.L2_52J2	X
Disp.L3_52J2	X
DDT Etapa 0	1
50BF ET0	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 03:41:29
Test End: 11-abr.-2019 03:41:38
User Name:
Manager:
Company:

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

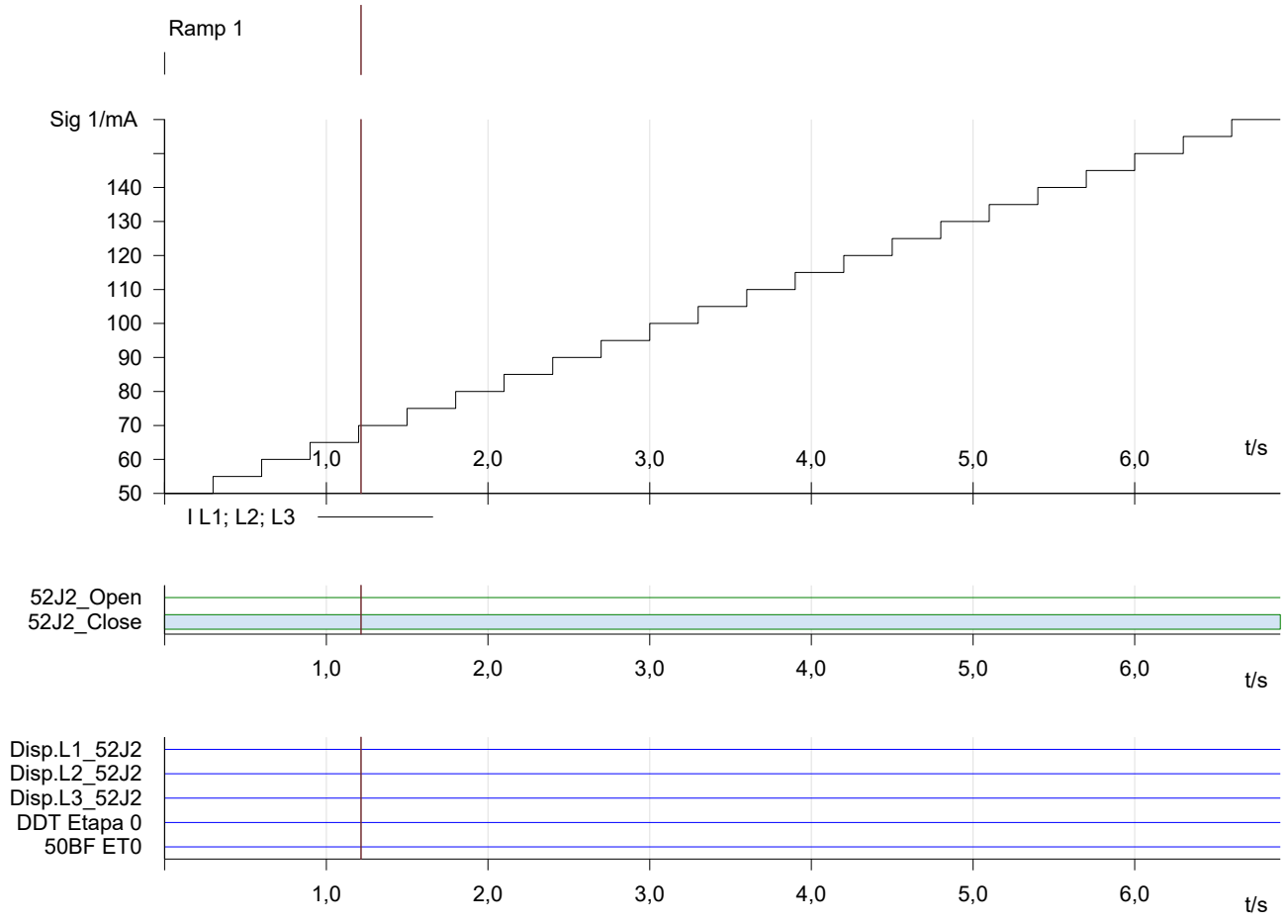
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

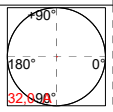
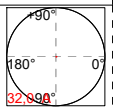
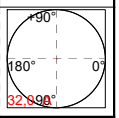
Test State:
Test passed

Group end:12.1 Verificacion Pickup_End Fault

Group:12.2 Operacion End Fault

12.2.1 Operacion End Fault_L1:

Test Settings

State	Prefalla	Falla L1+52J2 Open	Post Falla
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
52J2_Open	1	1	0
52J2_Close	0	0	0
Max. State Time	3,000 s	100,0 ms	2,000 s
Trigger Logic		AND	
50BF ET0		1	
User interaction	no	no	no
CMGPS trigger	no	no	no
IRIG-B/PTP trigger	no	no	no
Pulses / seconds	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no
Diagrams			

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:39:29	Test End:	11-abr.-2019 03:39:36
User Name:		Manager:	
Company:			

Test Results

Time Assessment

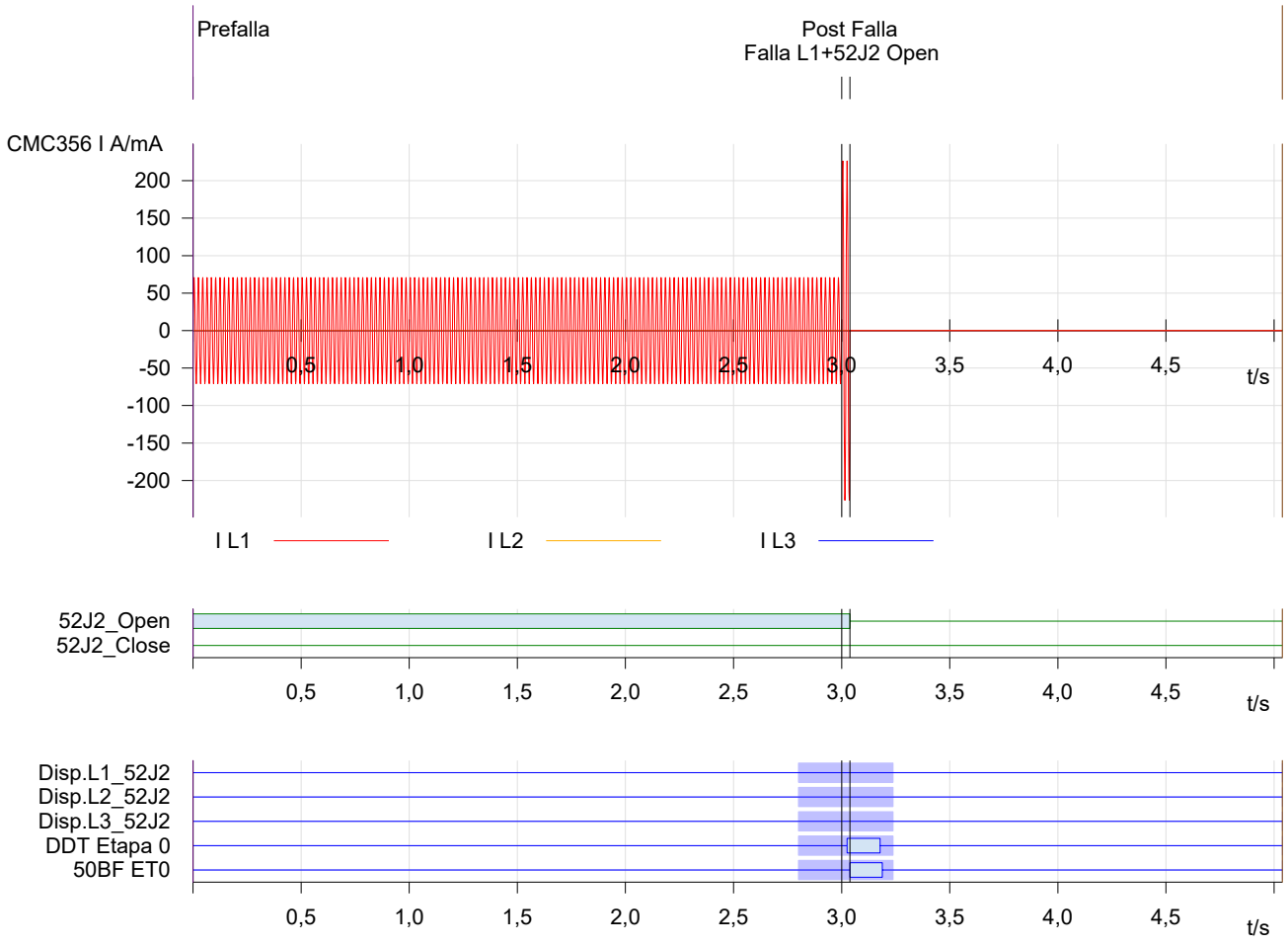
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L1+52J2 Open	Falla L1+52J2 Open	50BF ET0 0>1	50,00 ms	30,00 ms	30,00 ms	37,90 ms	-12,10 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L1+52J2 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms
Disp.L1_52J2	0	0	0
Disp.L2_52J2	0	0	0
Disp.L3_52J2	0	0	0
DDT Etapa 0	0	0	0
50BF ET0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a

Cursor 2	5,038 s	<none>	n/a
C2 - C1	5,038 s		n/a

Event recorder

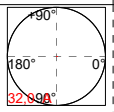
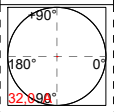
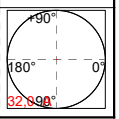
Time	Type	Signal name	Slope
3,025 s	Input	DDT Etapa 0	0>1
3,038 s	Input	50BF ET0	0>1
3,038 s	Output	52J2_Open	1>0
3,178 s	Input	DDT Etapa 0	1>0
3,188 s	Input	50BF ET0	1>0

Test State:

Test passed

12.2.2 Operacion End Fault_L2:

Test Settings

State	Prefalla	Falla L2+52J2 Open	Post Falla
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
52J2_Open	1	1	0
52J2_Close	0	0	0
Max. State Time	3,000 s	100,0 ms	2,000 s
Trigger Logic		AND	
50BF ET0		1	
User interaction	no	no	no
CMGPS trigger	no	no	no
IRIG-B/PTP trigger	no	no	no
Pulses / seconds	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no
Diagrams			

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:39:49	Test End:	11-abr.-2019 03:39:55
User Name:		Manager:	
Company:			

Test Results

Time Assessment

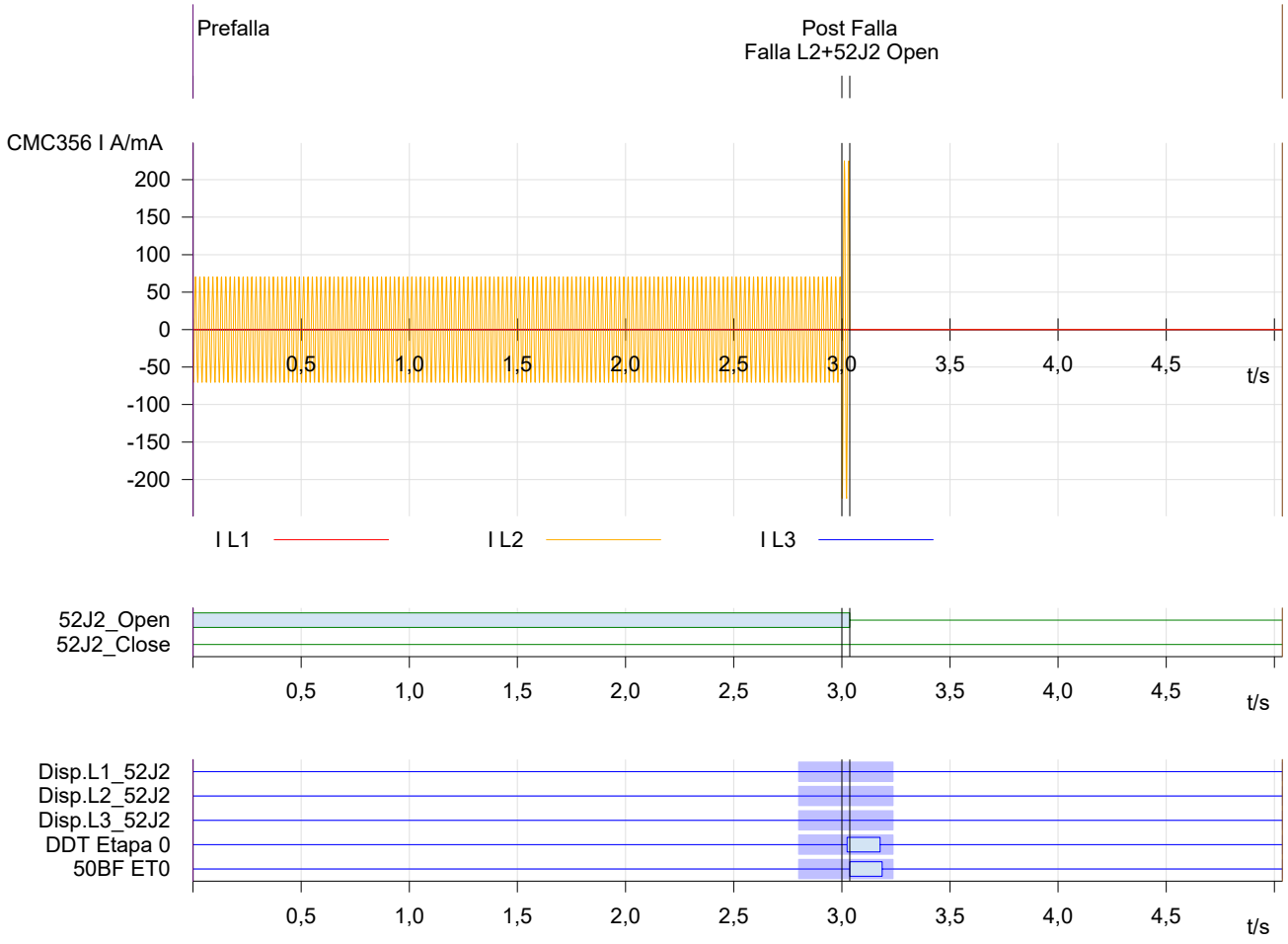
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L2+52J2 Open	Falla L2+52J2 Open	50BF ET0 0>1	50,00 ms	30,00 ms	30,00 ms	36,60 ms	-13,40 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L2+52J2 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms
Disp.L1_52J2	0	0	0
Disp.L2_52J2	0	0	0
Disp.L3_52J2	0	0	0
DDT Etapa 0	0	1	0
50BF ET0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a

Cursor 2	5,037 s	<none>	n/a
C2 - C1	5,037 s		n/a

Event recorder

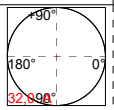
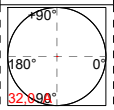
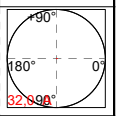
Time	Type	Signal name	Slope
3,024 s	Input	DDT Etapa 0	0>1
3,037 s	Input	50BF ET0	0>1
3,037 s	Output	52J2_Open	1>0
3,177 s	Input	DDT Etapa 0	1>0
3,187 s	Input	50BF ET0	1>0

Test State:

Test passed

12.2.3 Operacion End Fault_L3:

Test Settings

State	Prefalla	Falla L3+52J2 Open	Post Falla
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
52J2_Open	1	1	0
52J2_Close	0	0	0
Max. State Time	3,000 s	100,0 ms	2,000 s
Trigger Logic		AND	
DDT Etapa 0		1	
50BF ET0		1	
User interaction	no	no	no
CMGPS trigger	no	no	no
IRIG-B/PTP trigger	no	no	no
Pulses / seconds	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no
Diagrams			

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:40:07	Test End:	11-abr.-2019 03:40:14
User Name:		Manager:	
Company:			

Test Results

Time Assessment

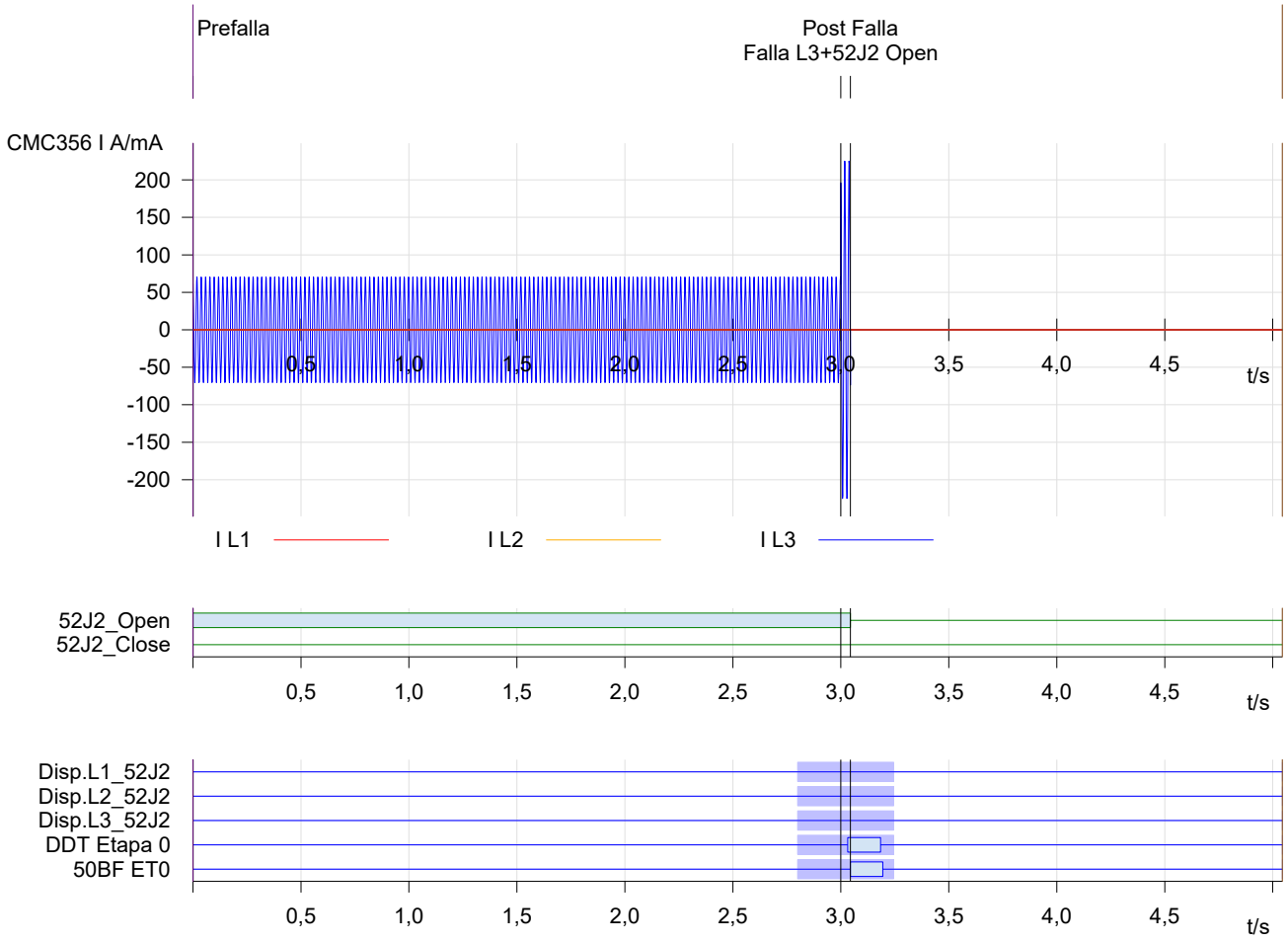
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L3+52J2 Open	Falla L3+52J2 Open	50BF ET0 0>1	50,00 ms	30,00 ms	30,00 ms	44,40 ms	-5,600 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L3+52J2 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms
Disp.L1_52J2	0	0	0
Disp.L2_52J2	0	0	0
Disp.L3_52J2	0	0	0
DDT Etapa 0	0	1	0
50BF ET0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	5,044 s	<none>	n/a
C2 - C1	5,044 s		n/a

Event recorder

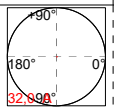
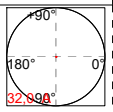
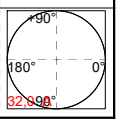
Time	Type	Signal name	Slope
3,032 s	Input	DDT Etapa 0	0>1
3,044 s	Input	50BF ET0	0>1
3,044 s	Output	52J2_Open	1>0
3,184 s	Input	DDT Etapa 0	1>0
3,194 s	Input	50BF ET0	1>0

Test State:

Test passed

12.2.4 Operacion End Fault_L123:

Test Settings

State	Prefalla	Falla L123+52J 2 Open	Post Falla
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
52J2_Open	1	1	0
52J2_Close	0	0	0
Max. State Time	3,000 s	100,0 ms	2,000 s
Trigger Logic		AND	
DDT Etapa 0		1	
50BF ET0		1	
User interaction	no	no	no
CMGPS trigger	no	no	no
IRIG-B/PTP trigger	no	no	no
Pulses / seconds	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no
Diagrams			

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:40:28	Test End:	11-abr.-2019 03:40:34
User Name:		Manager:	

Company:

Test Results

Time Assessment

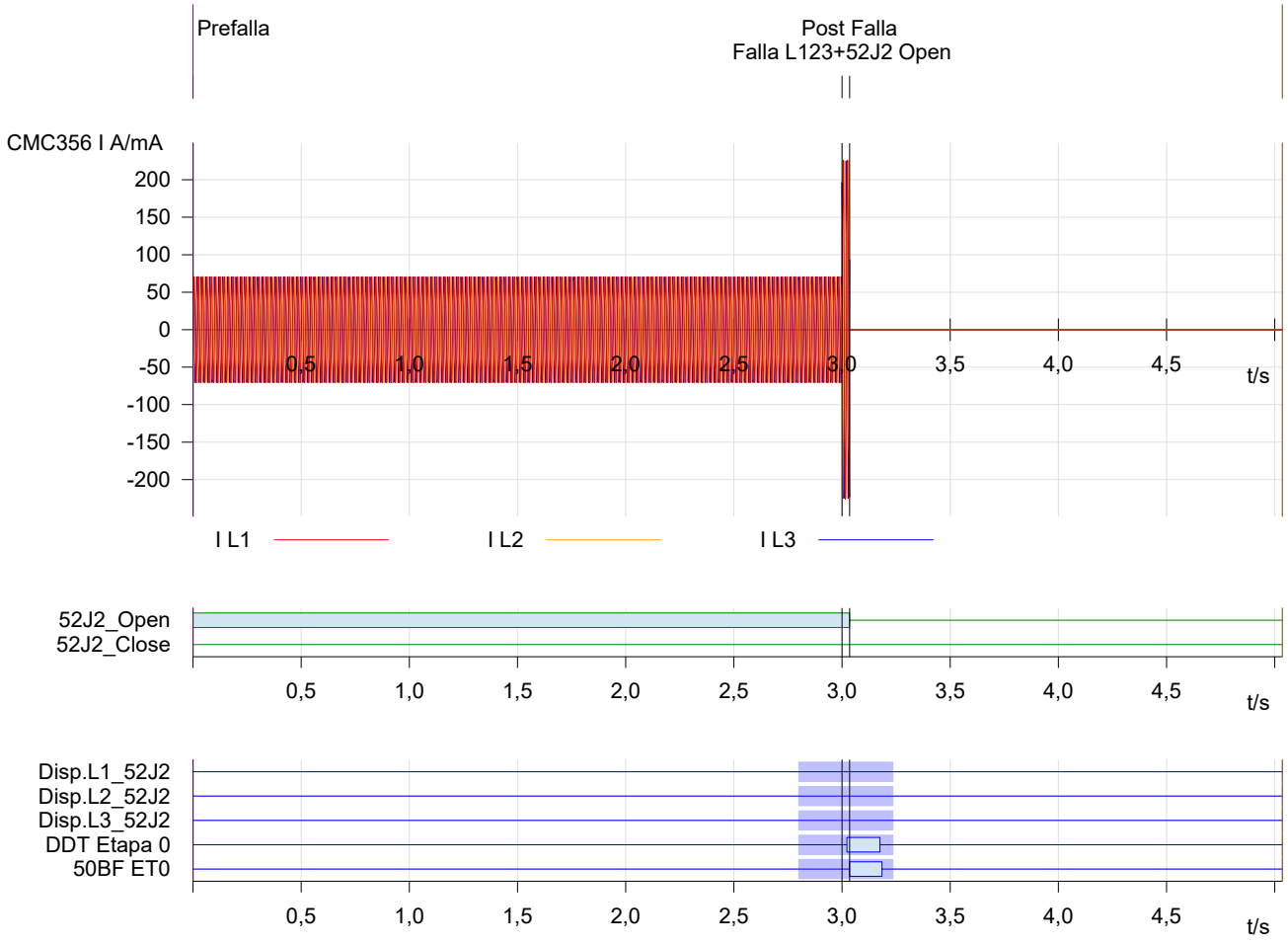
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L123+52J 2 Open	Falla L123+52J 2 Open	50BF ET0 0>1	50,00 ms	30,00 ms	30,00 ms	34,70 ms	-15,30 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L123+52J 2 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms
Disp.L1_52J2	0	0	0
Disp.L2_52J2	0	0	0
Disp.L3_52J2	0	0	0
DDT Etapa 0	0	1	0
50BF ET0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

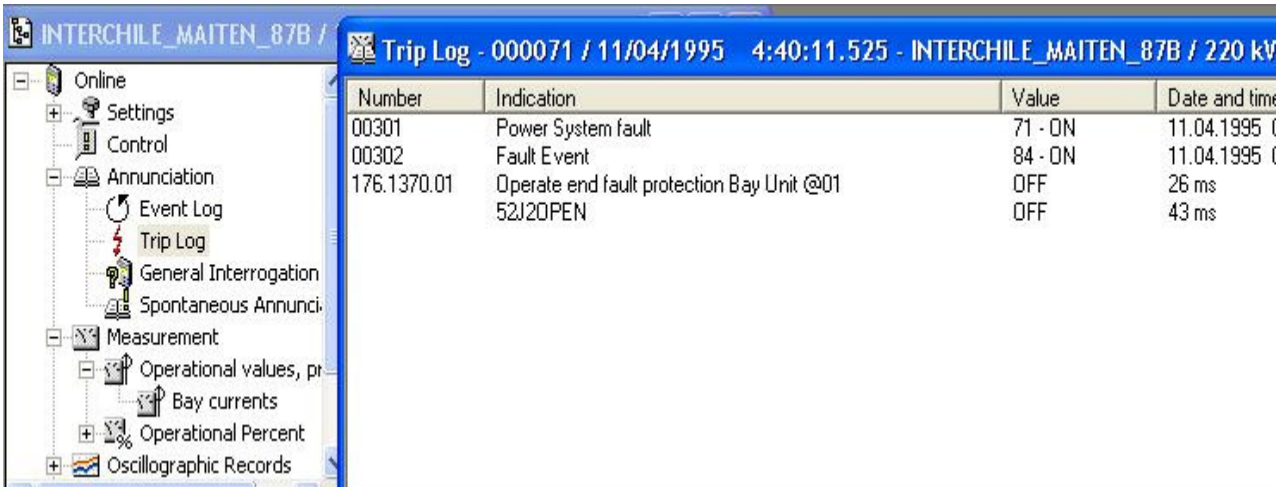
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	5,035 s	<none>	n/a
C2 - C1	5,035 s		n/a

Event recorder

Time	Type	Signal name	Slope
3,022 s	Input	DDT Etapa 0	0>1
3,035 s	Input	50BF ET0	0>1
3,035 s	Output	52J2_Open	1>0
3,175 s	Input	DDT Etapa 0	1>0
3,185 s	Input	50BF ET0	1>0

Test State:

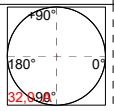
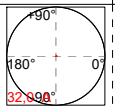
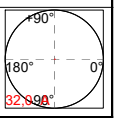
Test passed



12.2.5 Operacion End Fault_L123_CB Close:

Test Settings

State	Prefalla	Falla L123+52J 2 Open	Post Falla
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

52J2_Open	0	0	0
52J2_Close	1	1	0
Max. State Time	3,000 s	2,000 s	2,000 s
Trigger Logic			
User interaction	no	no	no
CMGPS trigger	no	no	no
IRIG-B/PTP trigger	no	no	no
Pulses / seconds	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no
Diagrams			

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 03:42:59	Test End:	11-abr.-2019 03:43:08
User Name:		Manager:	
Company:			

Test Results

Time Assessment

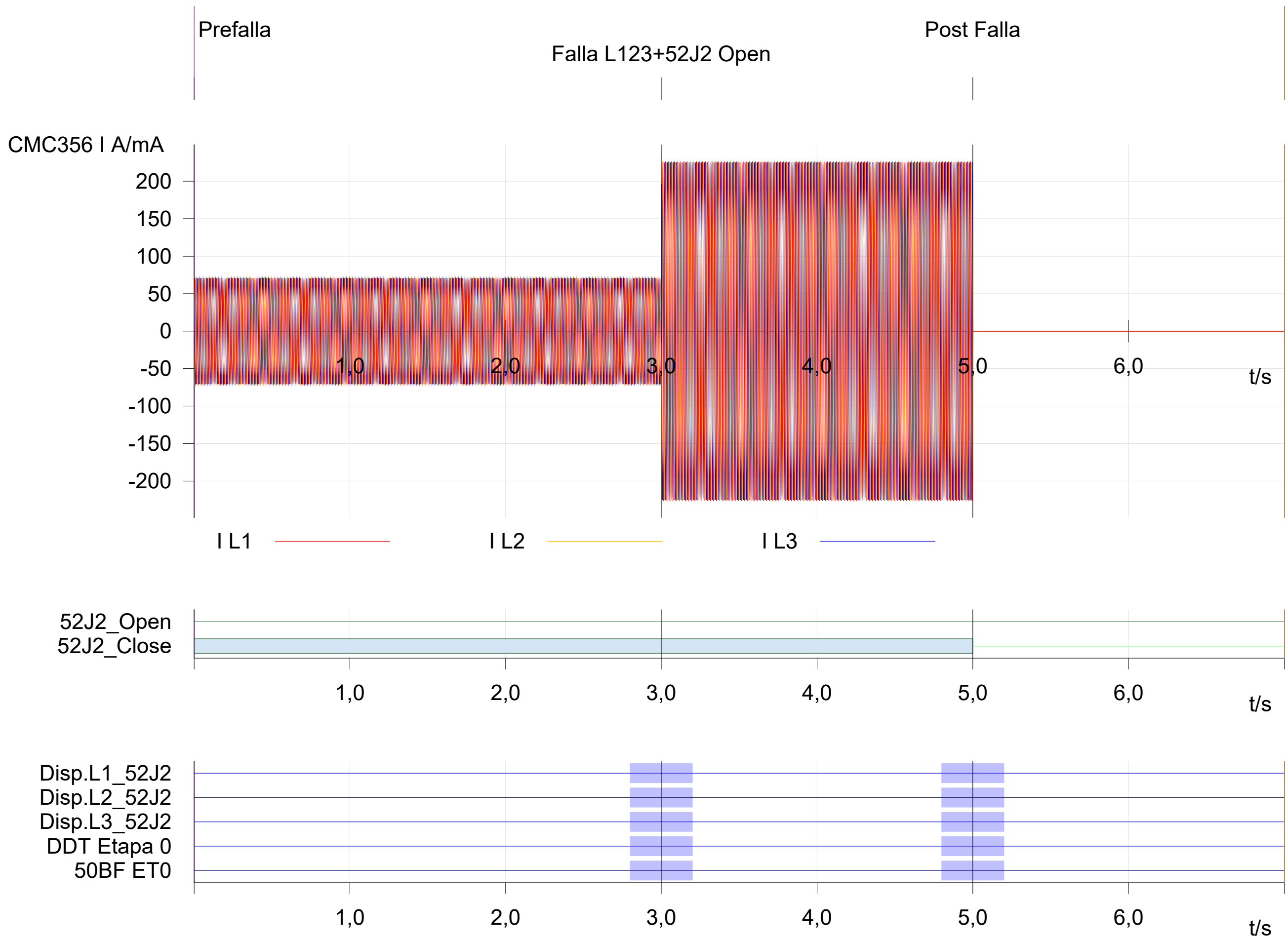
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
									o

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L123+52J 2 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms
Disp.L1_52J2	0	0	0
Disp.L2_52J2	0	0	0
Disp.L3_52J2	0	0	0
DDT Etapa 0	0	0	0
50BF ET0	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,000 s	<none>	n/a
C2 - C1	7,000 s		n/a

Event recorder

Time	Type	Signal name	Slope
5,000 s	Output	52J2_Close	1>0

Test State:
Test passed

Group end:12.2 Operacion End Fault

Group end:12. Operacion End Fault_50BF E0

ARCHIVO DE PRUEBAS OMICRON

AUDITORIA TECNICA DE EQUIPOS DE PROTECCIONES.

PROTECCION DE FALLA INTERRUPTOR - UNIDAD DE CAMPO 01 (52J3) EN S/E NUEVA MAITENCILLO
MODELO 7SS523, MARCA SIEMENS

INGEMA S. A		**CLIENTE**	
Probado por: Ing. Mario Aguilar	Revisado por: Ing. Antony Porras	Recibido por:	Aprobado por:
Fecha: 10-04-2019		Fecha:	Fecha:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Hadware

Test Equipment

Type	Serial Number
CMC356	MC355V

Hardware Check

Performed At	Result	Details
10-04-2019 23:32:27	Passed	

Group:1. Pickup 87B_ BU01_J3

1.1 Packup L1-L2-L3:

Test Settings

General

No. of ramp states: 1
Total steps per test: 41
Total time per test: 20,500 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	200,0 mA 0,00 ° 50,000 Hz
I L2	200,0 mA -120,00 ° 50,000 Hz
I L3	200,0 mA 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	200,0 mA
Sig 1 To	600,0 mA
Sig 1 Delta	10,00 mA
Sig 1 d/dt	20,00 mA/s
dt per Step	500,0 ms
Ramp Steps	41
Ramp Time	20,500s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	1
TRIP 87B-L2	1
TRIP 87B-L3	1
TRIP 87B-L1 B2	1
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	1
Step back	No
Delay Time	1,000 s

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	10-abr.-2019 23:52:09	Test End:	10-abr.-2019 23:52:18
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Arranque L1-L2-L3	Ramp 1	TRIP 87B-L1 0->1 and TRIP 87B-L2 0->1 and TRIP 87B-L3 0->1 and TRIP 87B-L1 B2 0->1 and TRIP 87B-L2 B2 0->1 and TRIP 87B-L3 B2 0->1	I L1; L2; L3	300,0 mA	310,0 mA	200,0 mA	200,0 mA	10,00 mA	+	27,90 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

Test Settings

General

No. of ramp states: 1
Total steps per test: 41
Total time per test: 20,500 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1; L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	200,0 mA 0,00 ° 50,000 Hz
I L2	200,0 mA -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	200,0 mA
Sig 1 To	600,0 mA
Sig 1 Delta	10,00 mA
Sig 1 d/dt	20,00 mA/s
dt per Step	500,0 ms
Ramp Steps	41
Ramp Time	20,500s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	1
TRIP 87B-L2	1
TRIP 87B-L3	1
TRIP 87B-L1 B2	1
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	1
Step back	No
Delay Time	1,000 s

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 10-abr.-2019 23:58:12
Test End: 10-abr.-2019 23:58:21
User Name:
Manager:
Company:

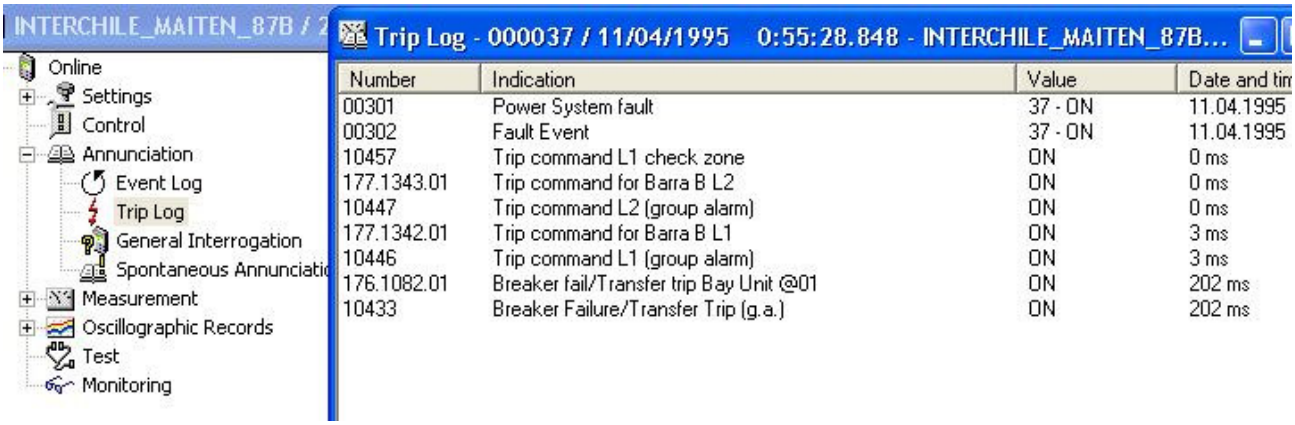
Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup L12	Ramp 1	TRIP 87B-L1 0->1 and TRIP 87B-L2 0->1 and TRIP 87B-L3 0->1 and TRIP 87B-L1 B2 0->1 and TRIP 87B-L2 B2 0->1 and TRIP 87B-L3 B2 0->1	I L1; L2	300,0 mA	310,0 mA	200,0 mA	200,0 mA	10,00 mA	+	27,40 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed



1.3 Packup L2-L3:

Test Settings

General

No. of ramp states: 1
Total steps per test: 41
Total time per test: 20,500 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	200,0 mA -120,00 ° 50,000 Hz

I L3	200,0 mA 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	200,0 mA
Sig 1 To	600,0 mA
Sig 1 Delta	10,00 mA
Sig 1 d/dt	20,00 mA/s
dt per Step	500,0 ms
Ramp Steps	41
Ramp Time	20,500s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	1
TRIP 87B-L2	1
TRIP 87B-L3	1
TRIP 87B-L1 B2	1
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	1
Step back	No
Delay Time	1,000 s

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	10-abr.-2019 23:58:47	Test End:	10-abr.-2019 23:58:55
User Name:		Manager:	
Company:			

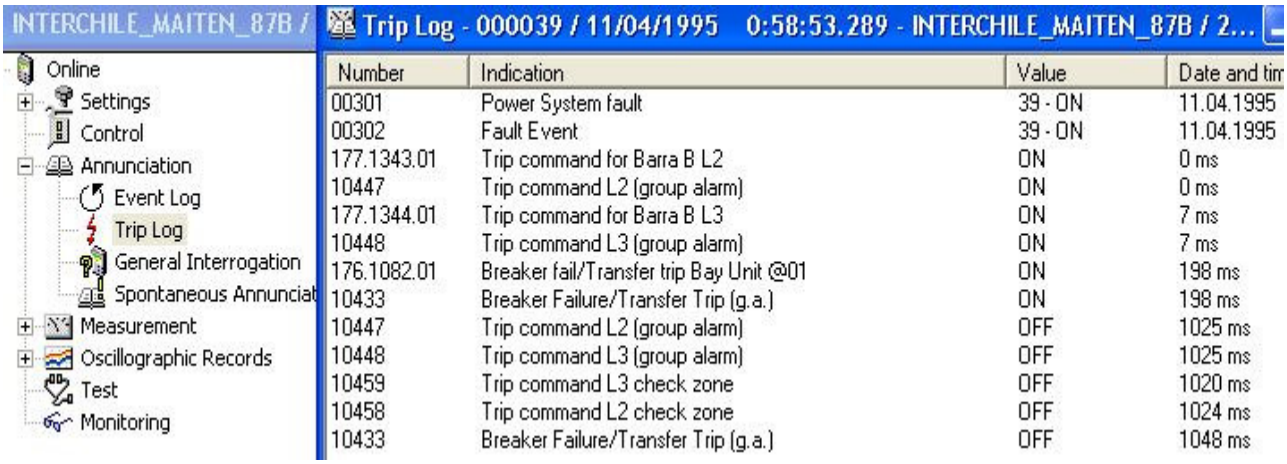
Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup L23	Ramp 1	TRIP 87B-L1 0->1 and TRIP 87B-L2 0->1 and TRIP 87B-L3 0->1 and TRIP 87B-L1 B2 0->1 and TRIP 87B-L2 B2 0->1 and TRIP 87B-L3 B2 0->1	I L2; L3	300,0 mA	310,0 mA	200,0 mA	200,0 mA	10,00 mA	+	25,50 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed



1.4 Packup L3-L1:

Test Settings

General

No. of ramp states: 1
Total steps per test: 41
Total time per test: 20,500 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L3; L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	200,0 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	200,0 mA 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	200,0 mA
Sig 1 To	600,0 mA
Sig 1 Delta	10,00 mA
Sig 1 d/dt	20,00 mA/s
dt per Step	500,0 ms
Ramp Steps	41
Ramp Time	20,500s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	1
TRIP 87B-L2	1
TRIP 87B-L3	1
TRIP 87B-L1 B2	1
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	X
Step back	No
Delay Time	1,000 s

Test Module

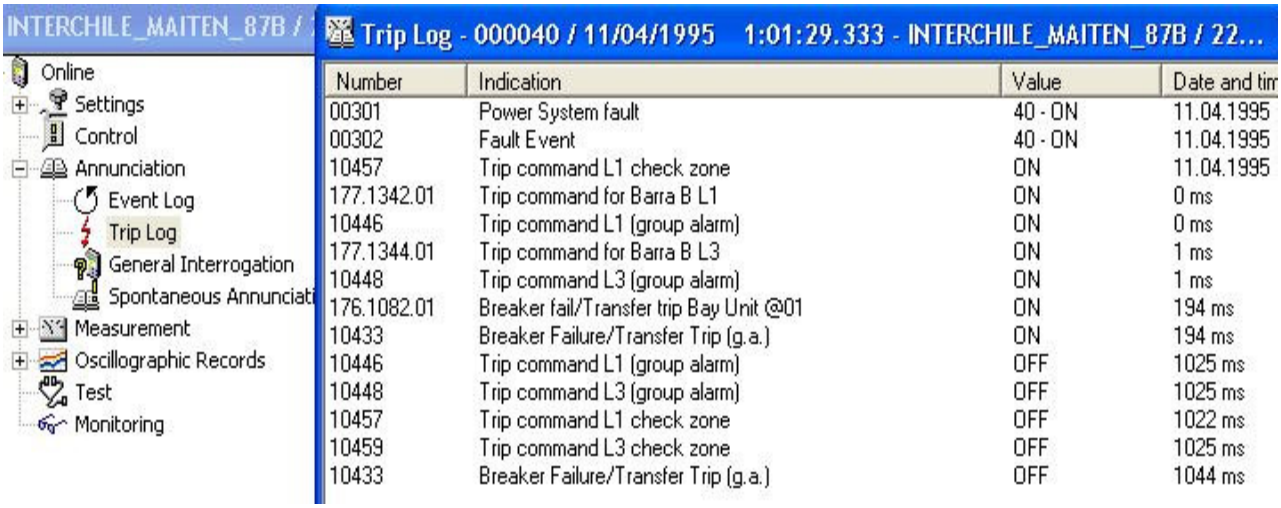
Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 00:01:23
Test End: 11-abr.-2019 00:01:32
User Name:
Manager:
Company:

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup L31	Ramp 1	TRIP 87B-L1 0->1 and TRIP 87B-L2 0->1 and TRIP 87B-L3 0->1	I L3; L1	300,0 mA	310,0 mA	200,0 mA	200,0 mA	10,00 mA	+	30,70 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed



Number	Indication	Value	Date and tim
00301	Power System fault	40 - ON	11.04.1995
00302	Fault Event	40 - ON	11.04.1995
10457	Trip command L1 check zone	ON	11.04.1995
177.1342.01	Trip command for Barra B L1	ON	0 ms
10446	Trip command L1 (group alarm)	ON	0 ms
177.1344.01	Trip command for Barra B L3	ON	1 ms
10448	Trip command L3 (group alarm)	ON	1 ms
176.1082.01	Breaker fail/Transfer trip Bay Unit @01	ON	194 ms
10433	Breaker Failure/Transfer Trip (g.a.)	ON	194 ms
10446	Trip command L1 (group alarm)	OFF	1025 ms
10448	Trip command L3 (group alarm)	OFF	1025 ms
10457	Trip command L1 check zone	OFF	1022 ms
10459	Trip command L3 check zone	OFF	1025 ms
10433	Breaker Failure/Transfer Trip (g.a.)	OFF	1044 ms

1.5 Packup L1:

Test Settings

General

No. of ramp states: 1
Total steps per test: 41
Total time per test: 20,500 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	200,0 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From **Sig 1 To** **Sig 1 Delta** **Sig 1 d/dt**	200,0 mA 600,0 mA 10,00 mA 20,00 mA/s
dt per Step **Ramp Steps** **Ramp Time**	500,0 ms 41 20,500s
Trigger	Bin
Trigger Logic **TRIP 87B-L1**	AND 1

TRIP 87B-L2	1
TRIP 87B-L3	1
TRIP 87B-L1 B2	1
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	1
Step back	No
Delay Time	1,000 s

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 00:06:53	Test End:	11-abr.-2019 00:07:02
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup L1	Ramp 1	TRIP 87B-L1 0->1 and TRIP 87B-L2 0->1 and TRIP 87B-L3 0->1 and TRIP 87B-L1 B2 0->1 and TRIP 87B-L2 B2 0->1 and TRIP 87B-L3 B2 0->1	I L1	300,0 mA	310,0 mA	300,0 mA	300,0 mA	10,00 mA	+	29,10 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

1.6 Packup L2:

Test Settings

General

No. of ramp states:	1
Total steps per test:	41
Total time per test:	20,500 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	200,0 mA -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	200,0 mA
Sig 1 To	600,0 mA
Sig 1 Delta	10,00 mA
Sig 1 d/dt	20,00 mA/s
dt per Step	500,0 ms
Ramp Steps	41
Ramp Time	20,500s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	1
TRIP 87B-L2	1
TRIP 87B-L3	1
TRIP 87B-L1 B2	1
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	1
Step back	No
Delay Time	1,000 s

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 00:05:50	Test End:	11-abr.-2019 00:05:58
User Name:		Manager:	
Company:			

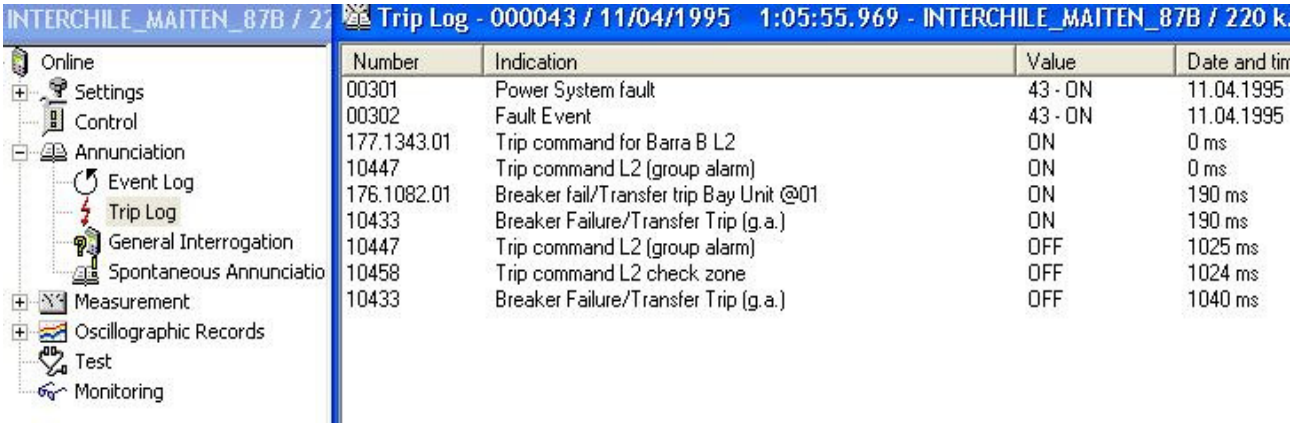
Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup L2	Ramp 1	TRIP 87B-L1 0->1 and TRIP 87B-L2 0->1 and TRIP 87B-L3 0->1 and TRIP 87B-L1 B2 0->1 and TRIP 87B-L2 B2 0->1 and TRIP 87B-L3 B2 0->1	I L2	300,0 mA	310,0 mA	300,0 mA	300,0 mA	10,00 mA	+	15,00 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed



1.7 Packup L3:

Test Settings

General

No. of ramp states: 1
Total steps per test: 41
Total time per test: 20,500 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz

I L3	200,0 mA 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	200,0 mA
Sig 1 To	600,0 mA
Sig 1 Delta	10,00 mA
Sig 1 d/dt	20,00 mA/s
dt per Step	500,0 ms
Ramp Steps	41
Ramp Time	20,500s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	1
TRIP 87B-L2	1
TRIP 87B-L3	1
TRIP 87B-L1 B2	1
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	1
Step back	No
Delay Time	1,000 s

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 00:07:55	Test End:	11-abr.-2019 00:08:04
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup L3	Ramp 1	TRIP 87B-L1 0->1 and TRIP 87B-L2 0->1 and TRIP 87B-L3 0->1 and TRIP 87B-L1 B2 0->1 and TRIP 87B-L2 B2 0->1 and TRIP 87B-L3 B2 0->1	I L3	300,0 mA	310,0 mA	300,0 mA	300,0 mA	10,00 mA	+	31,50 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

Group end:1. Pickup 87B_ BU01_J3

Group:2. Verificacion Medida Fase L1

2.1 Inyeccion 25% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:17:14	Test End:	11-abr.-2019 00:17:24
User Name:		Manager:	
Company:			

Test Results

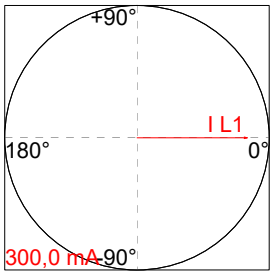
Title: Verificacion de Canal de Medida 25% Fase A

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	250,0 mA	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,250A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

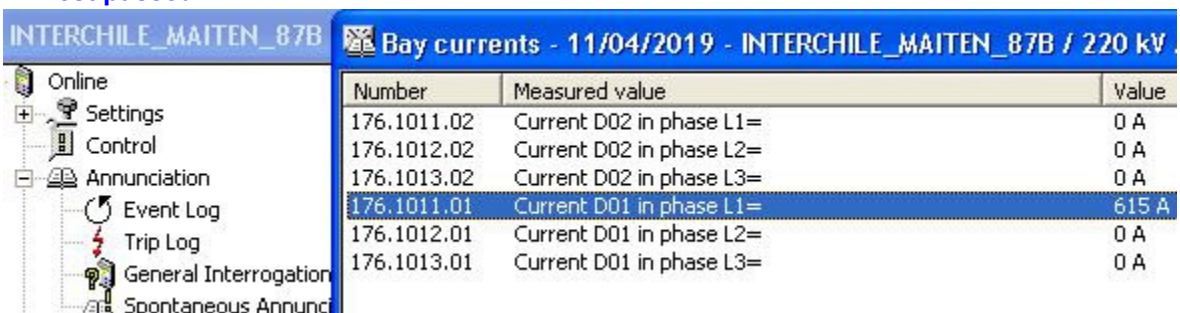
Passed 11-abr.-2019 00:17:19

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



2.2 Inyeccion 50% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:17:55	Test End:	11-abr.-2019 00:19:03
User Name:		Manager:	
Company:			

Test Results

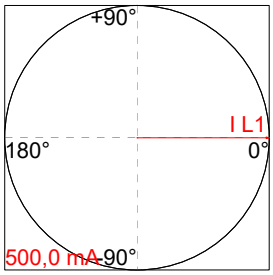
Title: Verificacion de Medida al 50% Fase A

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	500,0 mA	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,500A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

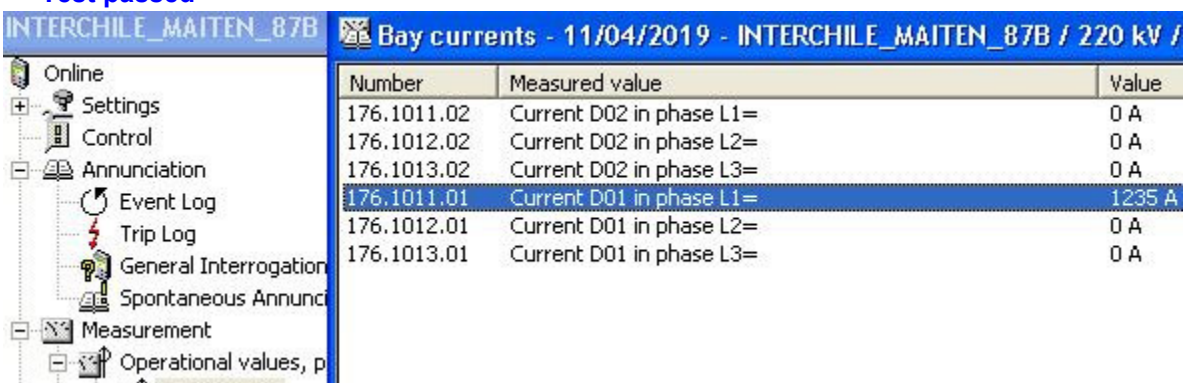
Passed 11-abr.-2019 00:18:31

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



2.3 Inyeccion 100% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:19:30	Test End:	11-abr.-2019 00:20:09
User Name:		Manager:	
Company:			

Test Results

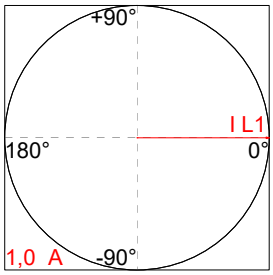
Title: Verificacion de Medida al 100% Fase A

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	1,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	1,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

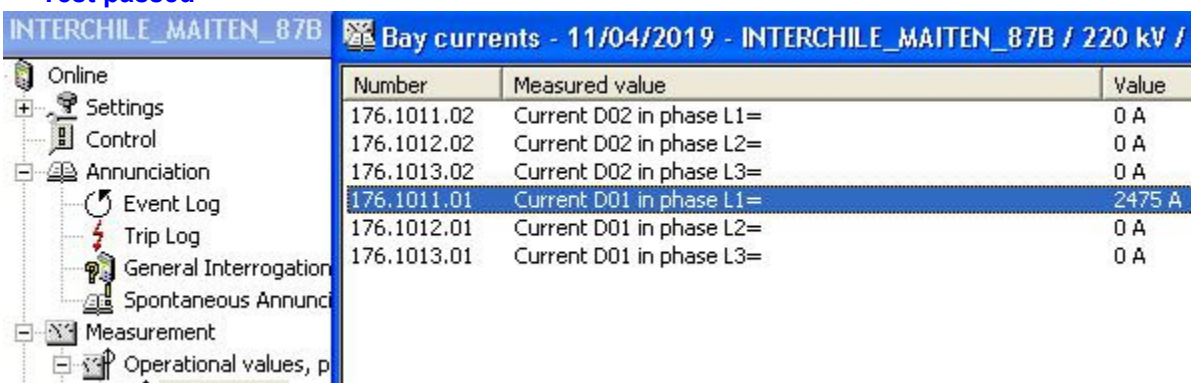
Passed 11-abr.-2019 00:19:40

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:2. Verificacion Medida Fase L1

Group:3. Verificacion Medida Fase L2

3.1 Inyeccion 25% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:20:41	Test End:	11-abr.-2019 00:21:31
User Name:		Manager:	
Company:			

Test Results

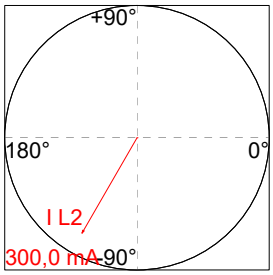
Title: Verificacion Medida al 25% Fase B

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	250,0 mA	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,250A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

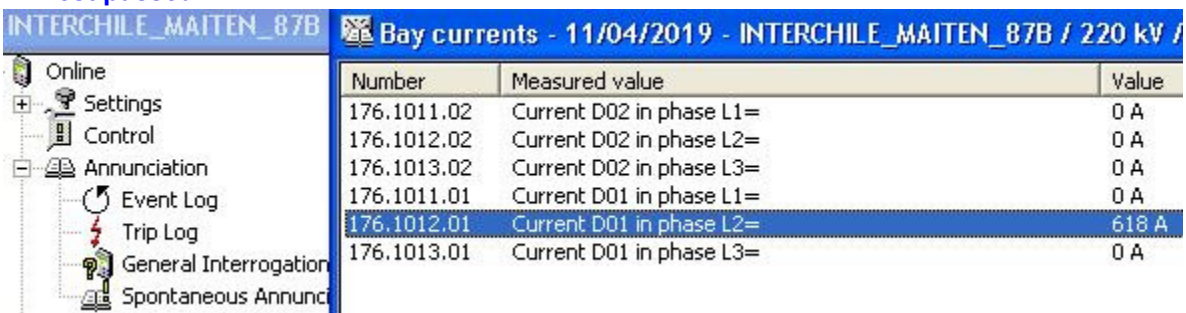
Passed 11-abr.-2019 00:20:48

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



3.2 Inyeccion 50% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:21:56	Test End:	11-abr.-2019 00:22:38
User Name:		Manager:	
Company:			

Test Results

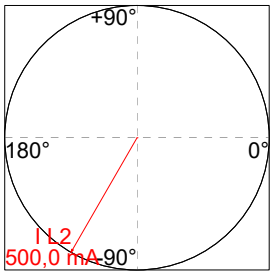
Title: Verificacion de Medidas al 50% Fase B

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	500,0 mA	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,500A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

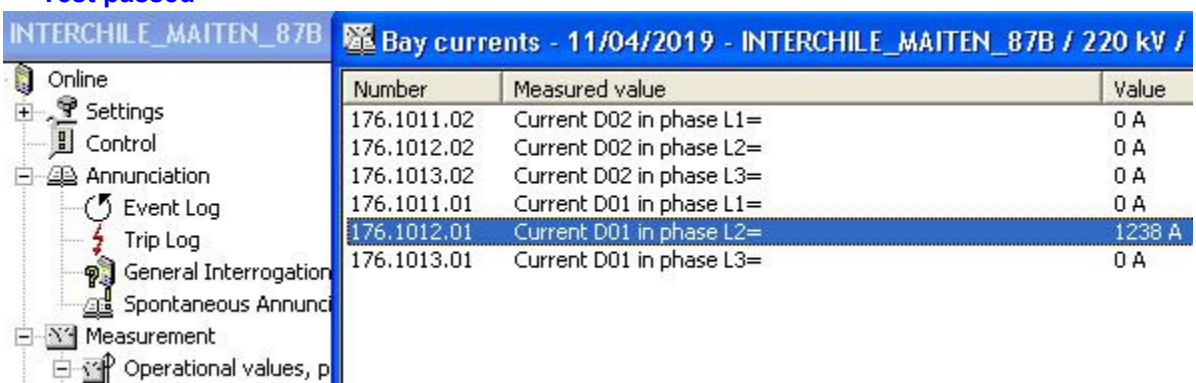
Passed 11-abr.-2019 00:22:05

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



3.3 Inyeccion 100% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:23:08	Test End:	11-abr.-2019 00:23:59
User Name:		Manager:	
Company:			

Test Results

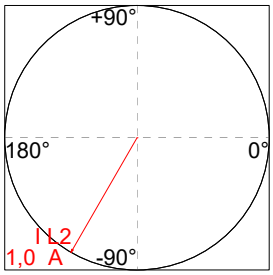
Title: Verificacion de Medidas al 100% Fase B

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	1,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	1,000A	-120,00°
I L3	0,000A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

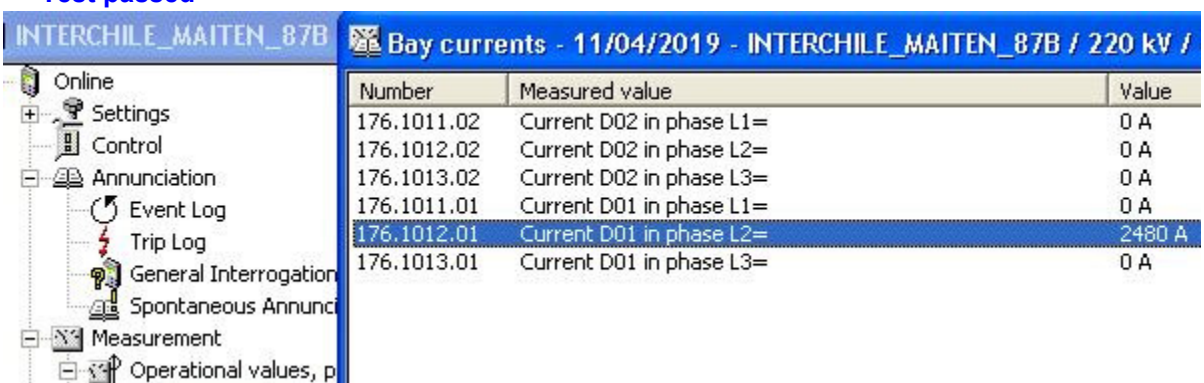
Passed 11-abr.-2019 00:23:25

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:3. Verificacion Medida Fase L2

Group:4. Verificacion Medida Fase L3

4.1 Inyeccion 25% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:24:48	Test End:	11-abr.-2019 00:25:56
User Name:		Manager:	
Company:			

Test Results

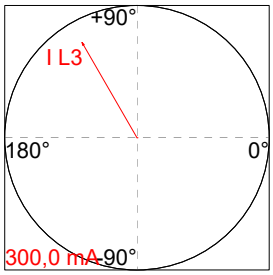
Title: Verificacion de Medidas al 25% Fase C

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	250,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,250A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

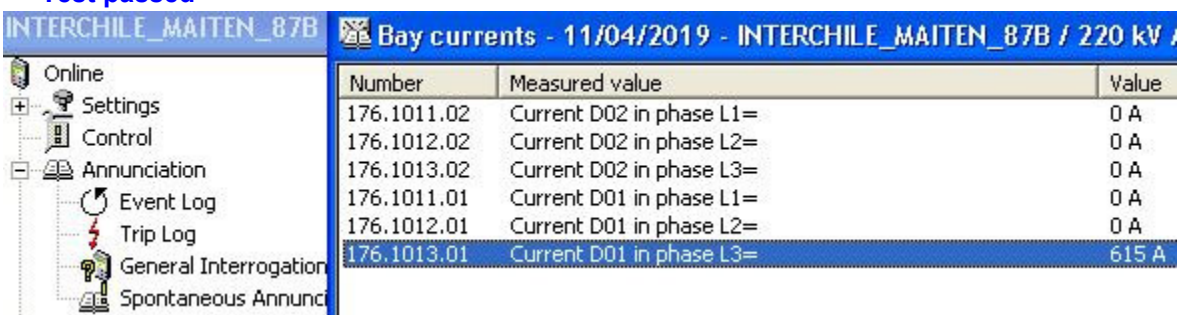
Passed 11-abr.-2019 00:24:59

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



4.2 Inyeccion 50% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:26:32	Test End:	11-abr.-2019 00:27:12
User Name:		Manager:	
Company:			

Test Results

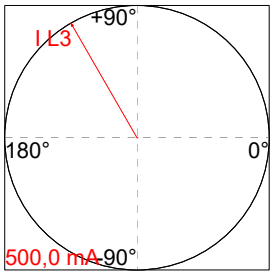
Title: Verificacion de Medidas al 50% Fase C

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	500,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,500A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

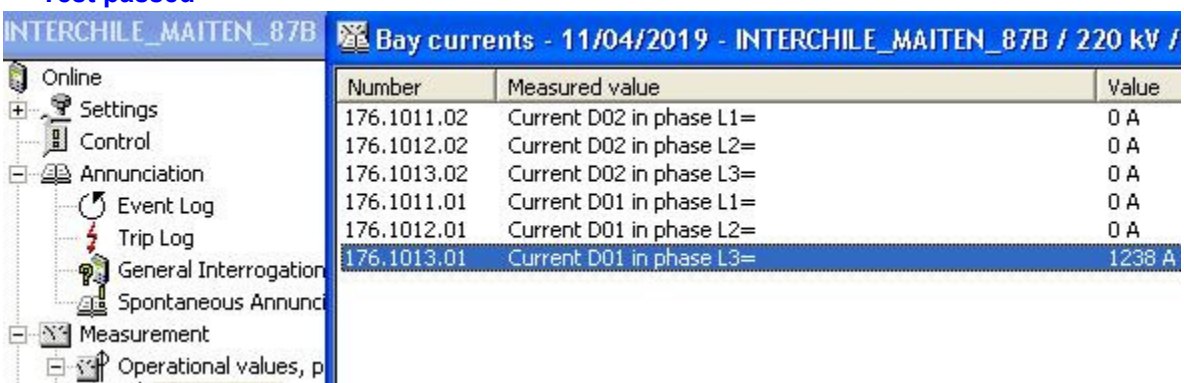
Passed 11-abr.-2019 00:26:41

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



4.3 Inyeccion 100% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:27:41	Test End:	11-abr.-2019 00:28:31
User Name:		Manager:	
Company:			

Test Results

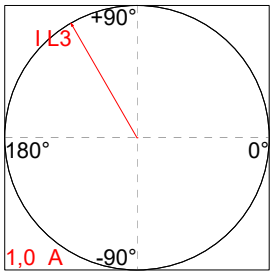
Title: Verificacion de medida al 100% Fase C

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	1,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	1,000A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

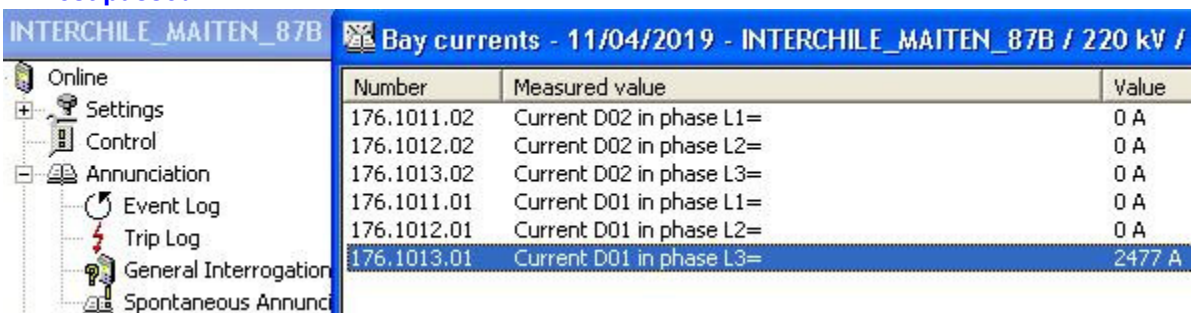
Passed 11-abr.-2019 00:27:53

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:4. Verificacion Medida Fase L3

Group:5. Verificacion Medida Fases L123

5.1 Inyeccion 25% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:29:00	Test End:	11-abr.-2019 00:29:43
User Name:		Manager:	
Company:			

Test Results

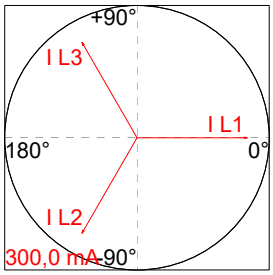
Title: Verificacion de Medidas al 25% Fase ABC

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	250,0 mA	0,00 °	50,000 Hz
	I L2	250,0 mA	-120,00 °	50,000 Hz
	I L3	250,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,250A	0,00°
I L2	0,250A	-120,00°
I L3	0,250A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

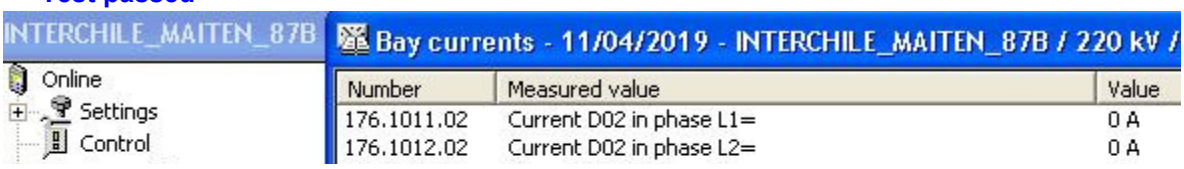
Passed 11-abr.-2019 00:29:11

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:30:52	Test End:	11-abr.-2019 00:31:26
User Name:		Manager:	
Company:			

Test Results

Title: Verificacion de Medidas al 50% Fase ABC

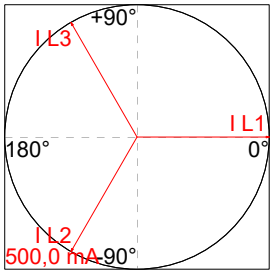
Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	500,0 mA	0,00 °	50,000 Hz
	I L2	500,0 mA	-120,00 °	50,000 Hz

	I L3	500,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,500A	0,00°
I L2	0,500A	-120,00°
I L3	0,500A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L1	0	
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

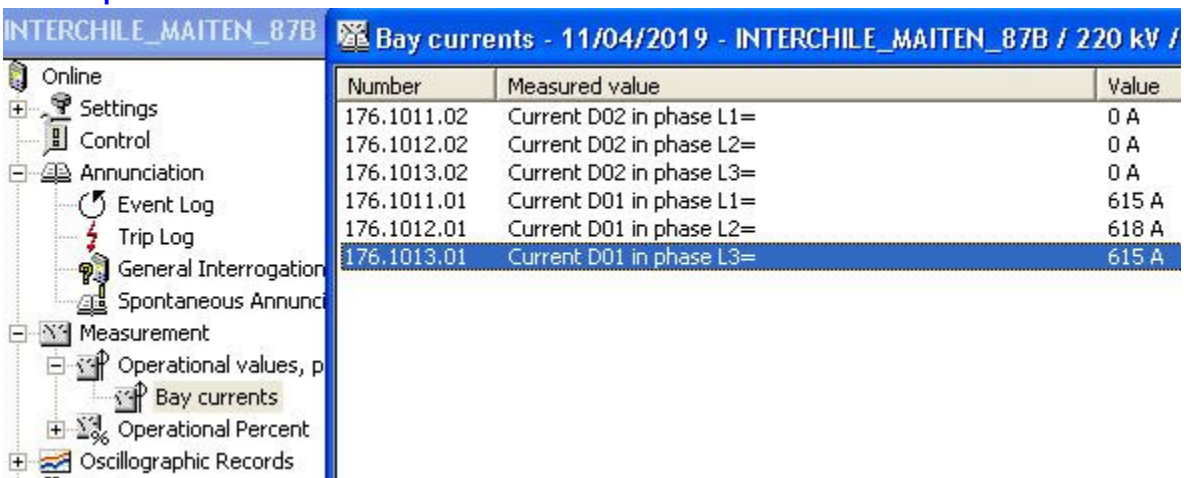
Passed 11-abr.-2019 00:30:37

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



5.3 Inyeccion 100% de Inominal:

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	14
Bay:	52J2	Bay address:	

Device:

Name/description:	BU@01_52J3	Manufacturer:	Siemens
Device type:	7SS522	Device address:	14
Serial/model number:	7SS523-0		
Additional info 1:	V3.3		
Additional info 2:			

Nominal Values:

f nom:	50,00 Hz	Number of phases:	3
V nom (secondary):	115,0 V	V primary:	230,0 kV
I nom (secondary):	1,000 A	I primary:	2,500 kA

Residual Voltage/Current Factors:

VLN / VN:	1,732	IN / I nom:	1,000

Limits:

V max:	200,0 V	I max:	50,00 A

Debounce/Deglitch Filters:

Debounce time:	3,000 ms	Deglitch time:	0,000 s

Overload Detection:

Suppression time:	50,00 ms

Other Device Properties:

Drop-out time:	20,00 ms

Test Object - Other RIO Functions

CB Configuration

Description	Name	Value
CB trip time	CB trip time	50,00 ms
CB close time	CB close time	100,00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20,00 %

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 00:31:54	Test End:	11-abr.-2019 00:32:34
User Name:		Manager:	
Company:			

Test Results

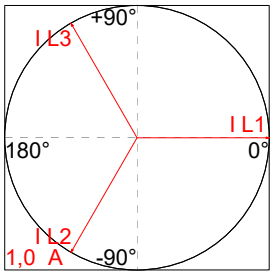
Title: Verificacion de Medidas al 100% Fase ABC

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	1,000 A	0,00 °	50,000 Hz
	I L2	1,000 A	-120,00 °	50,000 Hz
	I L3	1,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	1,000A	0,00°
I L2	1,000A	-120,00°
I L3	1,000A	120,00°



Binary Outputs

Name	State
Sal. bin. 1	0
Sal. bin. 2	0
Sal. bin. 3	0
Sal. bin. 4	0

Binary Inputs

Name	Slope	Time
TRIP 87B-L2	0	
TRIP 87B-L3	0	
A 86B	0	
TRIP 87B-L1 B2	0	
TRIP 87B-L2 B2	0	
TRIP 87B-L3 B2	0	
Overload	0	

Analog Inputs

VDCin	IDCin
n/a	n/a

Comment

Synchronized mode (Synchronization to external signal failed)

Assessment

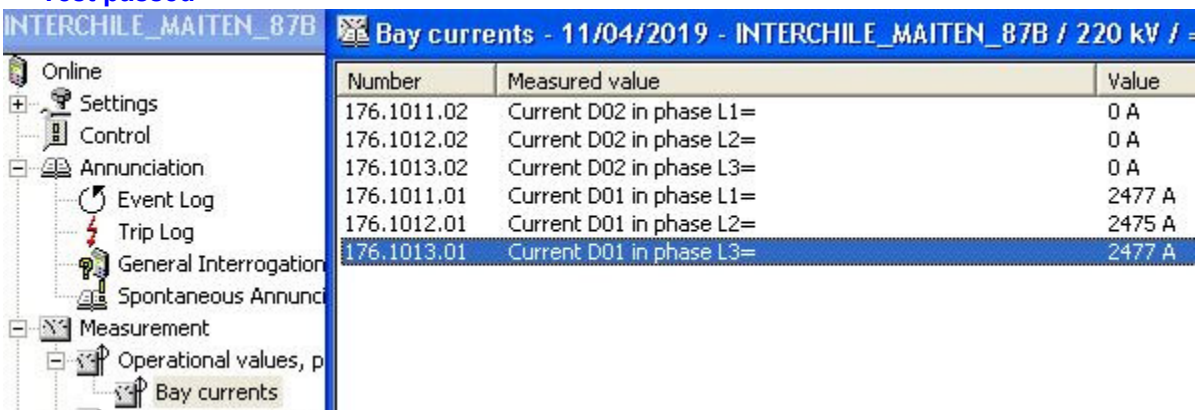
Passed 11-abr.-2019 00:32:01

Comment

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:5. Verificacion Medida Fases L123

Group:6. Verificacion Pickup 50BF Fase L1

6.1 Pickup con Arranque Fase L1:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	1
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	OR
TRIP 87B-L1	1
TRIP 87B-L2	X
TRIP 87B-L3	X
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	X
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 00:48:43
Test End: 11-abr.-2019 00:48:51
User Name:
Manager:
Company:

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L1	Ramp 1	TRIP 87B-L1 0->1	I L1	100,0 mA	105,0 mA	300,0 mA	300,0 mA	5,000 mA	+	61,00 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

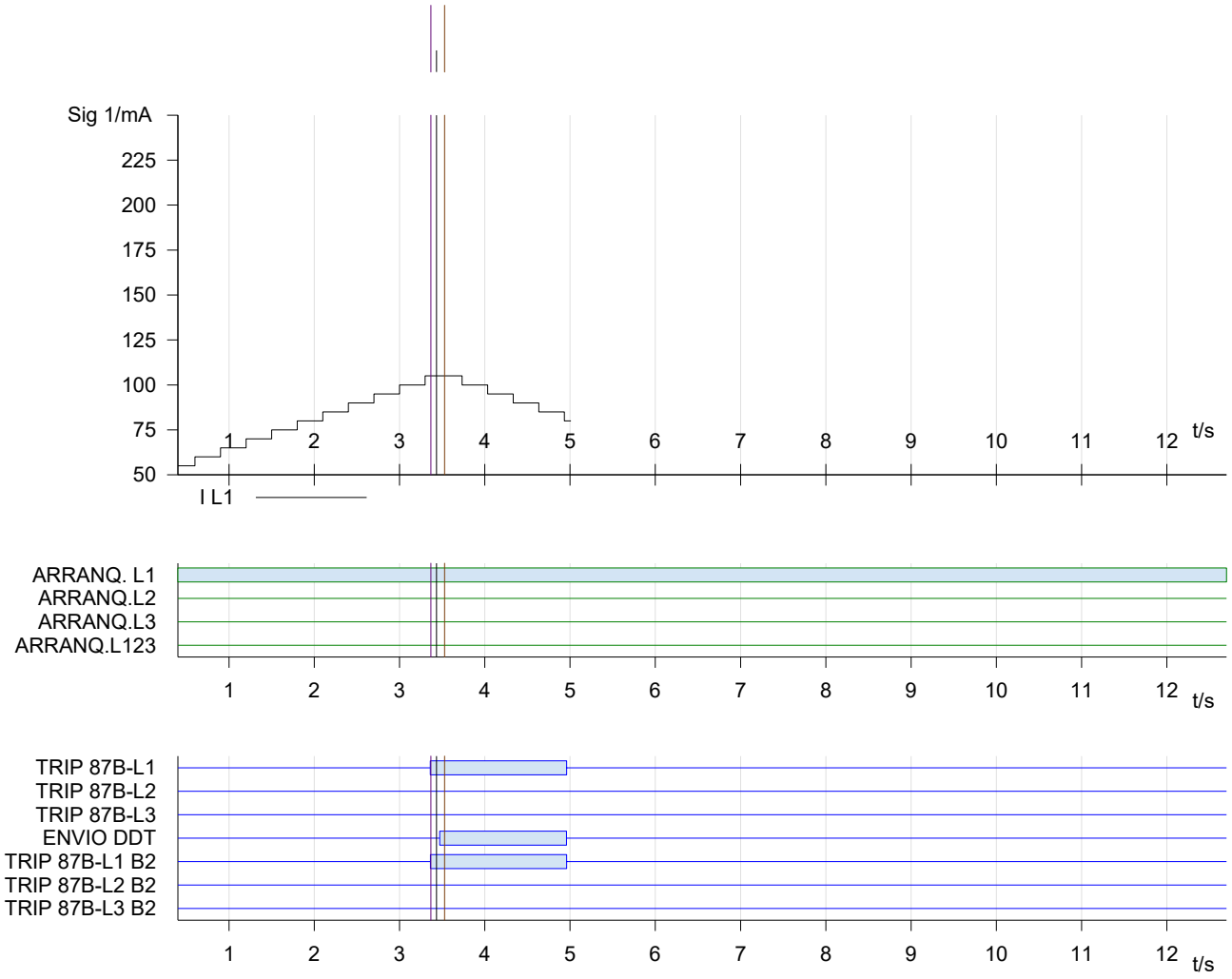
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
Drop-off/Pick-up	X/Y	Pickup_Fase L1	Pickup_Fase L1	0,9500	1,000			0,05000	+

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	3,368 s	<none>	n/a
Cursor 2	3,528 s	<none>	n/a
C2 - C1	160,4 ms		n/a

Test State:
Test passed

6.2 Pickup sin Arranque Fase L1:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	OR
TRIP 87B-L1	1
TRIP 87B-L2	X
TRIP 87B-L3	X
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	X
Step back	Yes

Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 00:49:41	Test End:	11-abr.-2019 00:49:50
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

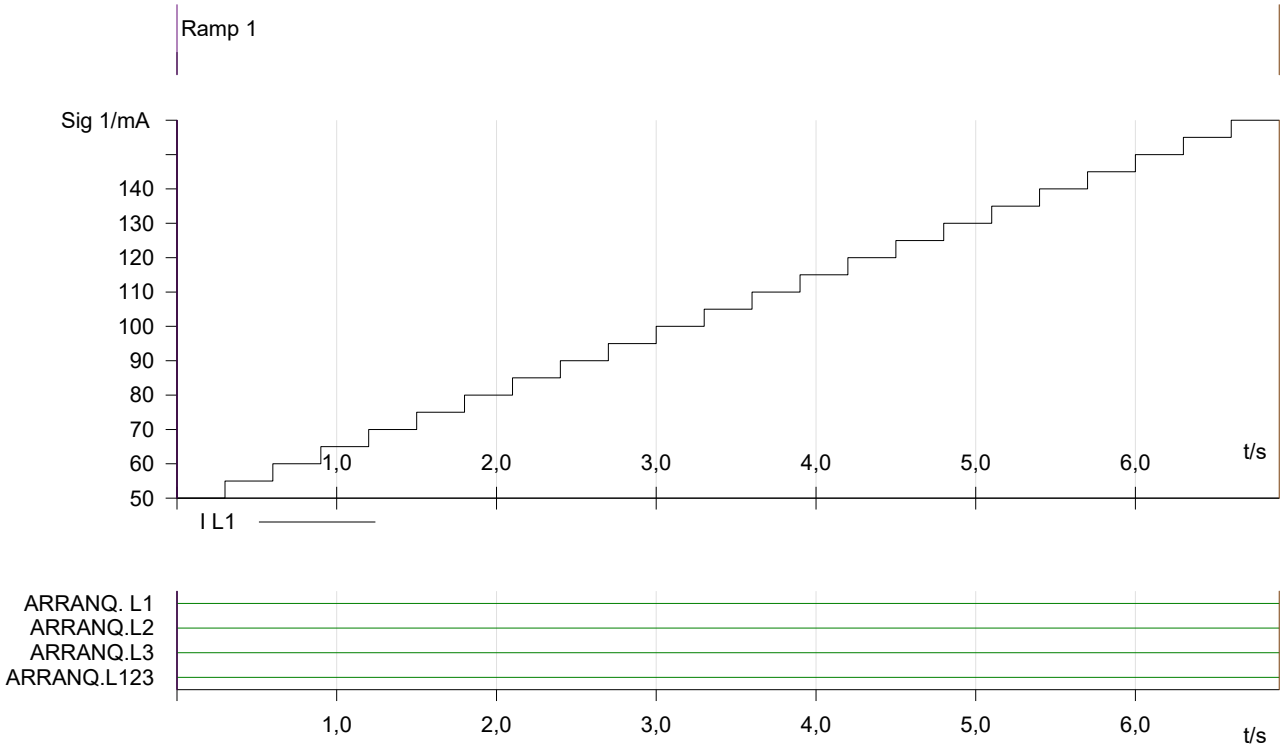
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

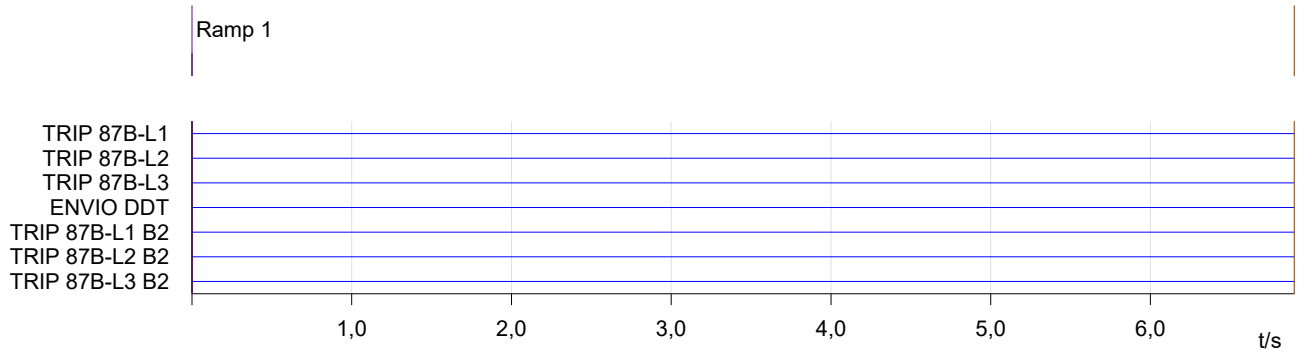
Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	6,900 s	<none>	n/a
C2 - C1	6,900 s		n/a

Test State:
Test passed

Group end:6. Verificacion Pickup 50BF Fase L1
Group:7. Verificacion Pickup 50BF Fase L2

6.1 Pickup con Arranque Fase L2:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s

ARRANQ. L1	0
ARRANQ.L2	1
ARRANQ.L3	0
ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	X
TRIP 87B-L2	1
TRIP 87B-L3	X
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	X
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 00:52:13	Test End:	11-abr.-2019 00:52:20
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	TRIP 87B-L2 0->1 and TRIP 87B-L2 B2 0->1	I L2	100,0 mA	105,0 mA	300,0 mA	300,0 mA	5,000 mA	+	58,50 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

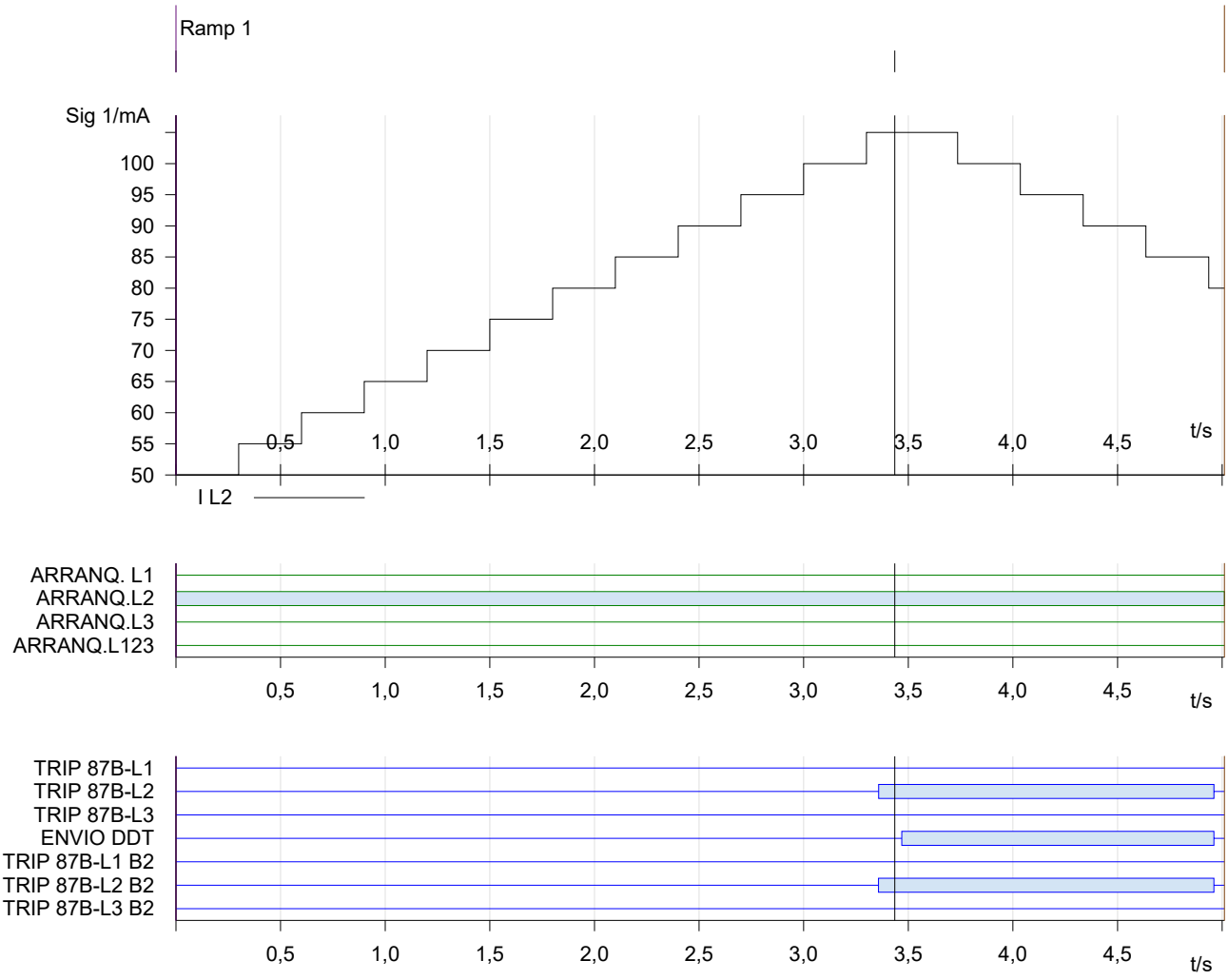
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
Drop-off/Pick-up	X/Y	Pickup_Fase L2	Pickup_Fase L2	0,9500	1,000			0,05000	+

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	5,011 s	<none>	n/a
C2 - C1	5,011 s		n/a

Test State:

Test passed

6.2 Pickup sin Arranque Fase L2:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	X
TRIP 87B-L2	1
TRIP 87B-L3	X
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 00:53:11	Test End:	11-abr.-2019 00:53:19
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

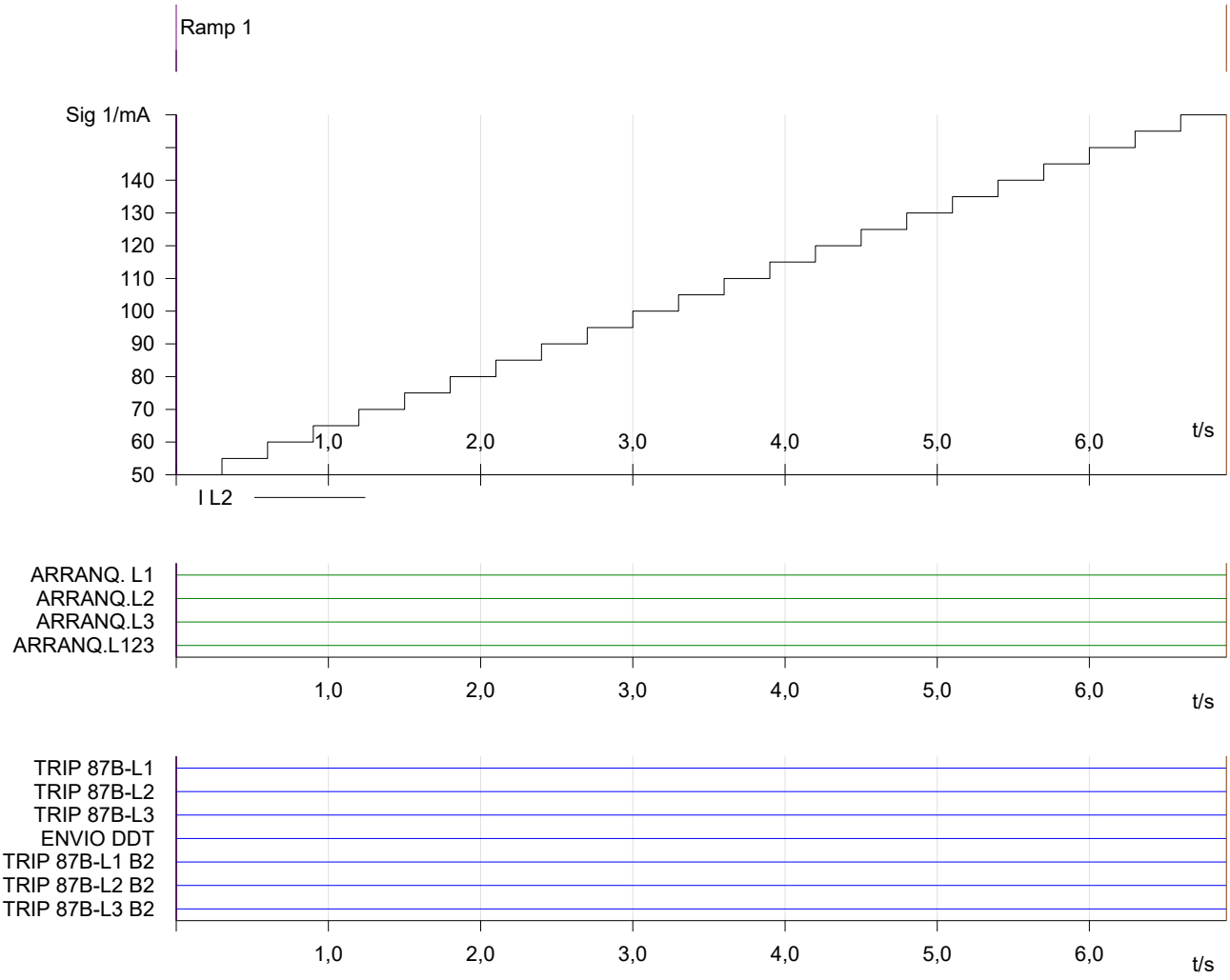
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	6,900 s	<none>	n/a
C2 - C1	6,900 s		n/a

Test State:
Test passed

- Group end:7. Verificacion Pickup 50BF Fase L2 -
- Group:8. Verificacion Pickup 50BF Fase L3 -

8.1 Pickup con Arranque Fase L3:

Test Settings

General

No. of ramp states:	1
Total steps per test:	23
Total time per test:	6,900 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	1
ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	X
TRIP 87B-L2	X
TRIP 87B-L3	1
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 00:55:20	Test End:	11-abr.-2019 00:55:27
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	TRIP 87B-L3 0->1 and TRIP 87B-L3 B2 0->1	I L3	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	60,20 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

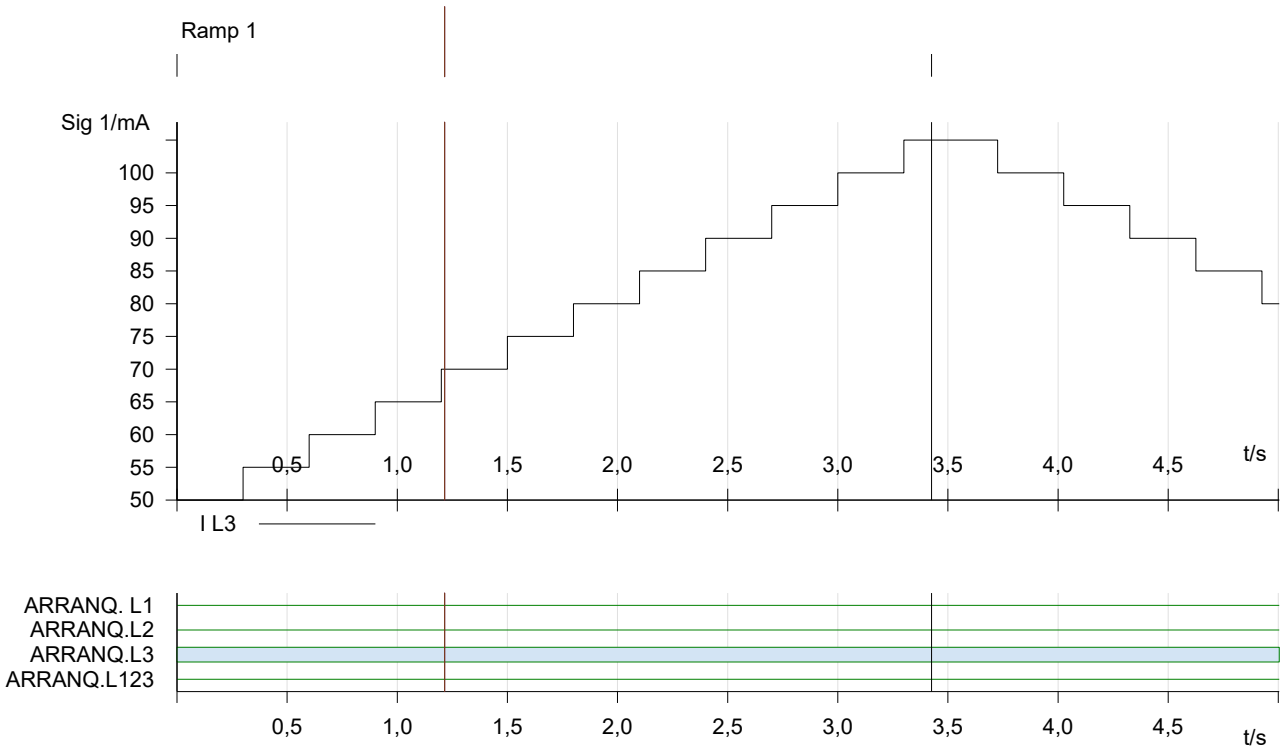
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
Drop-off/Pick-up	X/Y	Pickup_Fase L2	Pickup_Fase L2	0,9500	1,000			0,05000	+

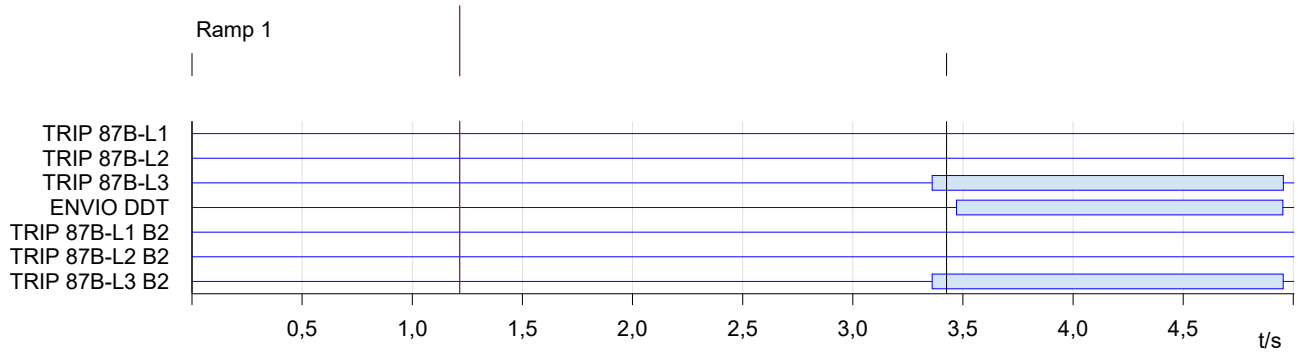
Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

	Time	Signal	Value
Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:
Test passed

8.2 Pickup sin Arranque Fase L3:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From **Sig 1 To** **Sig 1 Delta** **Sig 1 d/dt**	50,00 mA 160,0 mA 5,000 mA 16,67 mA/s
ARRANQ. L1 **ARRANQ.L2** **ARRANQ.L3**	0 0 0

ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	X
TRIP 87B-L2	X
TRIP 87B-L3	1
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 00:56:16	Test End:	11-abr.-2019 00:56:25
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

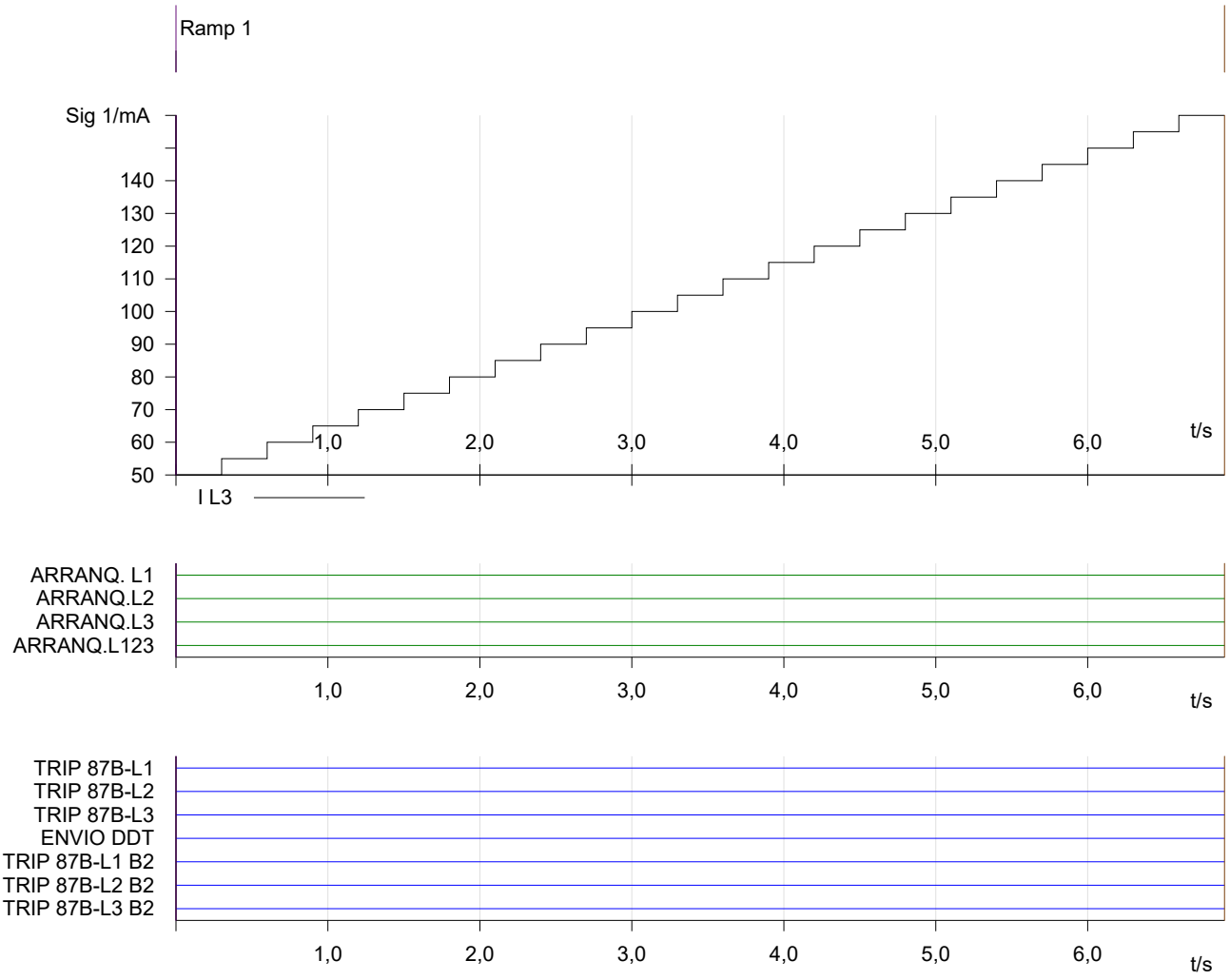
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	6,900 s	<none>	n/a
C2 - C1	6,900 s		n/a

Test State:

Test passed

Group end:8. Verificacion Pickup 50BF Fase L3

Group:9. Verificacion Pickup 50BF Fases L123

9.1 Pickup con Arranque Fases L123:

Test Settings

General

No. of ramp states:	1
Total steps per test:	23
Total time per test:	6,900 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
ARRANQ. L1	0
ARRANQ.L2	0
ARRANQ.L3	0
ARRANQ.L123	1
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	1
TRIP 87B-L2	1
TRIP 87B-L3	1
ENVIO DDT	X
TRIP 87B-L1 B2	1
TRIP 87B-L2 B2	1
TRIP 87B-L3 B2	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 00:58:27	Test End:	11-abr.-2019 00:58:34
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L123	Ramp 1	TRIP 87B-L3 0->1 and TRIP 87B-L1 B2 0->1 and TRIP 87B-L1 0->1 and TRIP 87B-L2 0->1 and TRIP 87B-L2 B2 0->1 and TRIP 87B-L3 B2 0->1	I L1; L2; L3	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	56,90 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

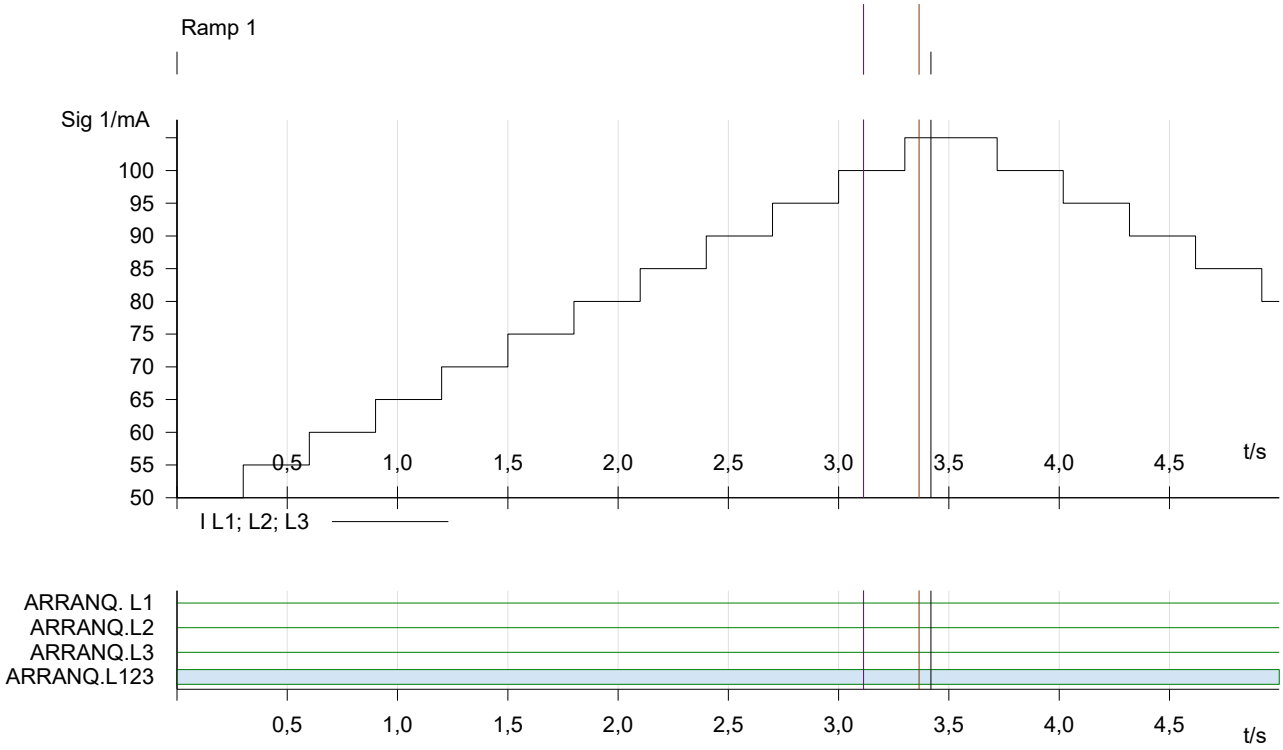
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

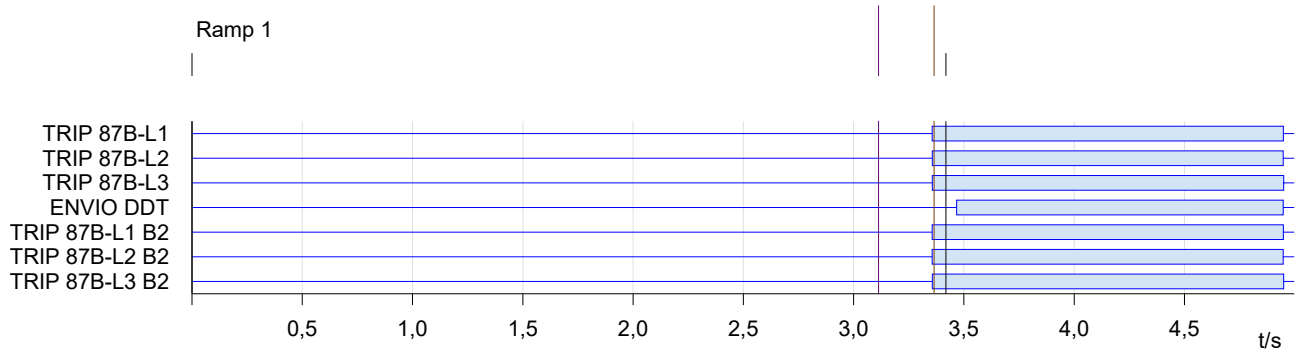
Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

	Time	Signal	Value
Cursor 1	3,113 s	<none>	n/a
Cursor 2	3,365 s	<none>	n/a
C2 - C1	251,4 ms		n/a

Test State:
Test passed

8.2 Pickup sin Arranque Fases L123:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From **Sig 1 To** **Sig 1 Delta** **Sig 1 d/dt**	50,00 mA 160,0 mA 5,000 mA 16,67 mA/s
ARRANQ. L1 **ARRANQ.L2** **ARRANQ.L3**	0 0 0

ARRANQ.L123	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
TRIP 87B-L1	1
TRIP 87B-L2	1
TRIP 87B-L3	1
ENVIO DDT	X
TRIP 87B-L1 B2	X
TRIP 87B-L2 B2	X
TRIP 87B-L3 B2	X
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 00:59:19	Test End:	11-abr.-2019 00:59:28
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

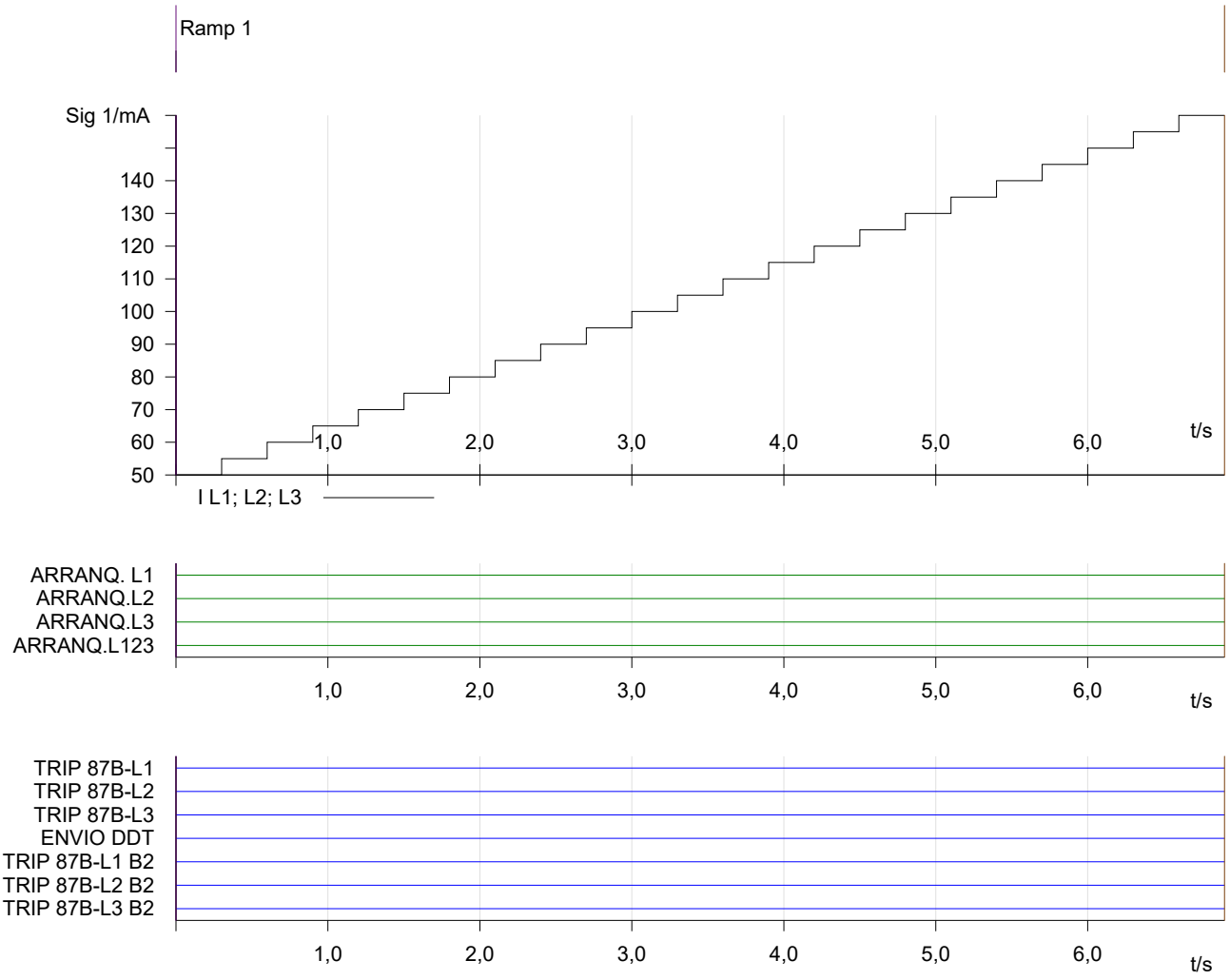
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	6,900 s	<none>	n/a
C2 - C1	6,900 s		n/a

Test State:
Test passed

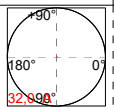
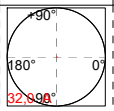
Group end:9. Verificacion Pickup 50BF Fases L123

Group:10. Operacion 50BF_J3 (T1)

10.1 Operacion 50BF_Fase L1 :

Test Settings

State	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1	Post-Falla 2
I L1	50,00 mA 0,00 °	160,0 mA 0,00 °	0,000 A 0,00 °	160,0 mA 0,00 °	0,000 A 0,00 °

I L1	50,000 Hz	50,000 Hz	50,000 Hz	50,000 Hz	50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	1	0
ARRANQ.L2	0	0	0	0	0
ARRANQ.L3	0	0	0	0	0
ARRANQ.L123	0	0	0	0	0
Max. State Time	3,000 s	3,000 s	1,000 s	100,0 ms	1,000 s
Trigger Logic				AND	OR
TRIP 87B-L1				1	1
TRIP 87B-L2				0	X
TRIP 87B-L3				0	X
TRIP 87B-L1 B2				1	X
User interaction	no	no	no	no	no
CMGPS trigger	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no
Pulses / seconds	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	50,00 ms	0,000 s
On trigger jump to test end	no	no	no	no	no
Diagrams					

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:04:08	Test End:	11-abr.-2019 01:04:16
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	TRIP 87B-L1 0>1	50,00 ms	30,00 ms	30,00 ms	66,30 ms	16,30 ms	+

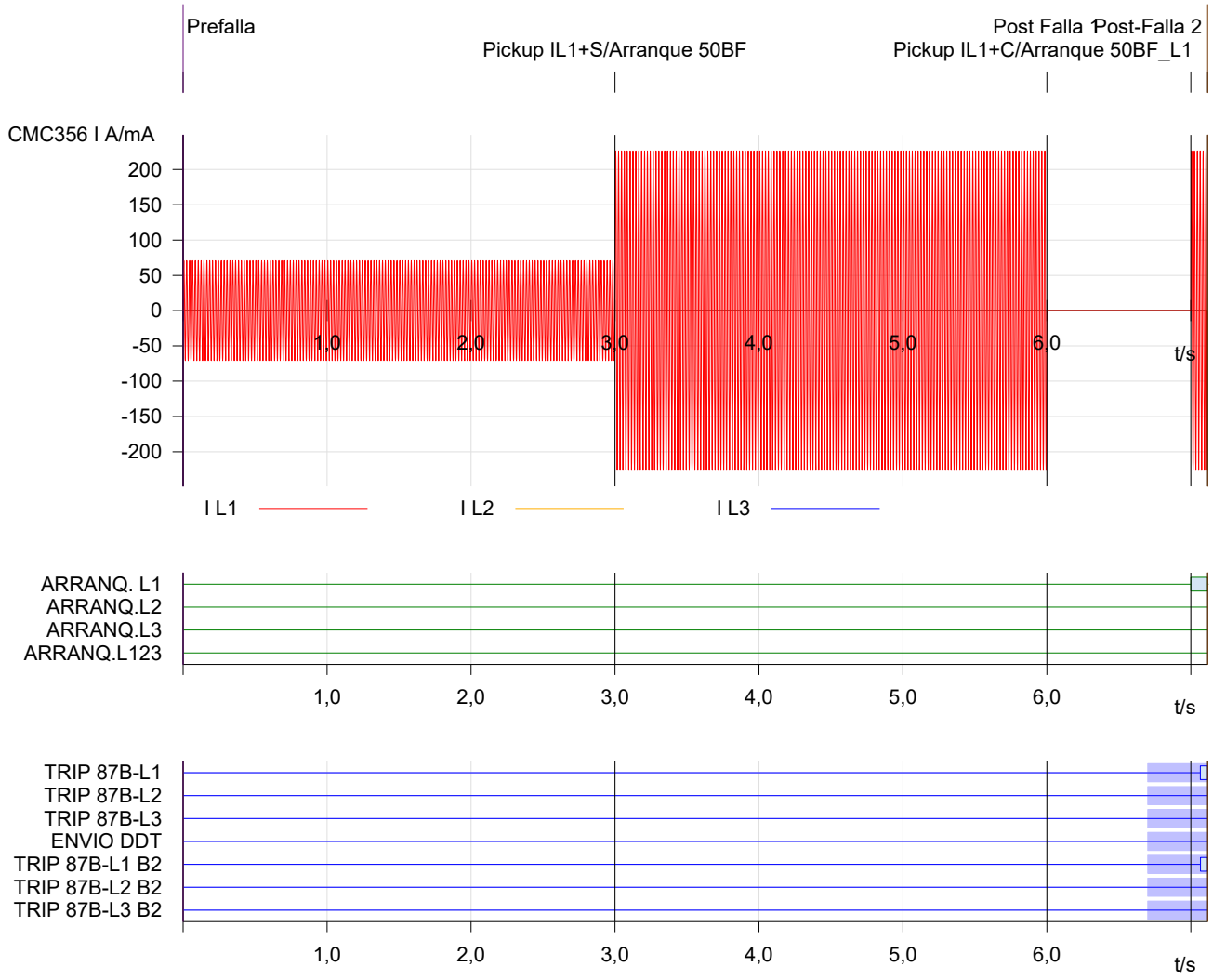
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1	Post-Falla 2
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	50,00 ms
TRIP 87B-L1	0	0	0	1	0
TRIP 87B-L2	0	0	0	0	0
TRIP 87B-L3	0	0	0	0	0

ENVIO DDT	0	0	0	0	0
TRIP 87B-L1 B2	0	0	0	1	0
TRIP 87B-L2 B2	0	0	0	0	0
TRIP 87B-L3 B2	0	0	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,117 s	<none>	n/a
C2 - C1	7,117 s		n/a

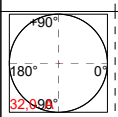
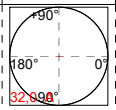
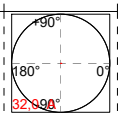
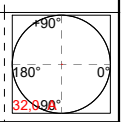
Event recorder

Time	Type	Signal name	Slope
7,000 s	Output	ARRANQ. L1	0>1
7,066 s	Input	TRIP 87B-L1	0>1
7,066 s	Input	TRIP 87B-L1 B2	0>1
7,116 s	Output	ARRANQ. L1	1>0

Test State:
Test passed

10.2 Operacion 50BF_Fase L2 :

Test Settings

State	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L2	Post-Falla 2
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	0	0
ARRANQ.L2	0	0	0	1	0
ARRANQ.L3	0	0	0	0	0
ARRANQ.L123	0	0	0	0	0
Max. State Time	3,000 s	2,000 s	100,0 ms	100,0 ms	1,000 s
Trigger Logic			OR	AND	
TRIP 87B-L2			1	1	
TRIP 87B-L2 B2			X	1	
User interaction	no	no	no	no	no
CMGPS trigger	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no
Pulses / seconds	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	yes	no	no
Diagrams					

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:09:50	Test End:	11-abr.-2019 01:09:58
User Name:		Manager:	
Company:			

Test Results

Time Assessment

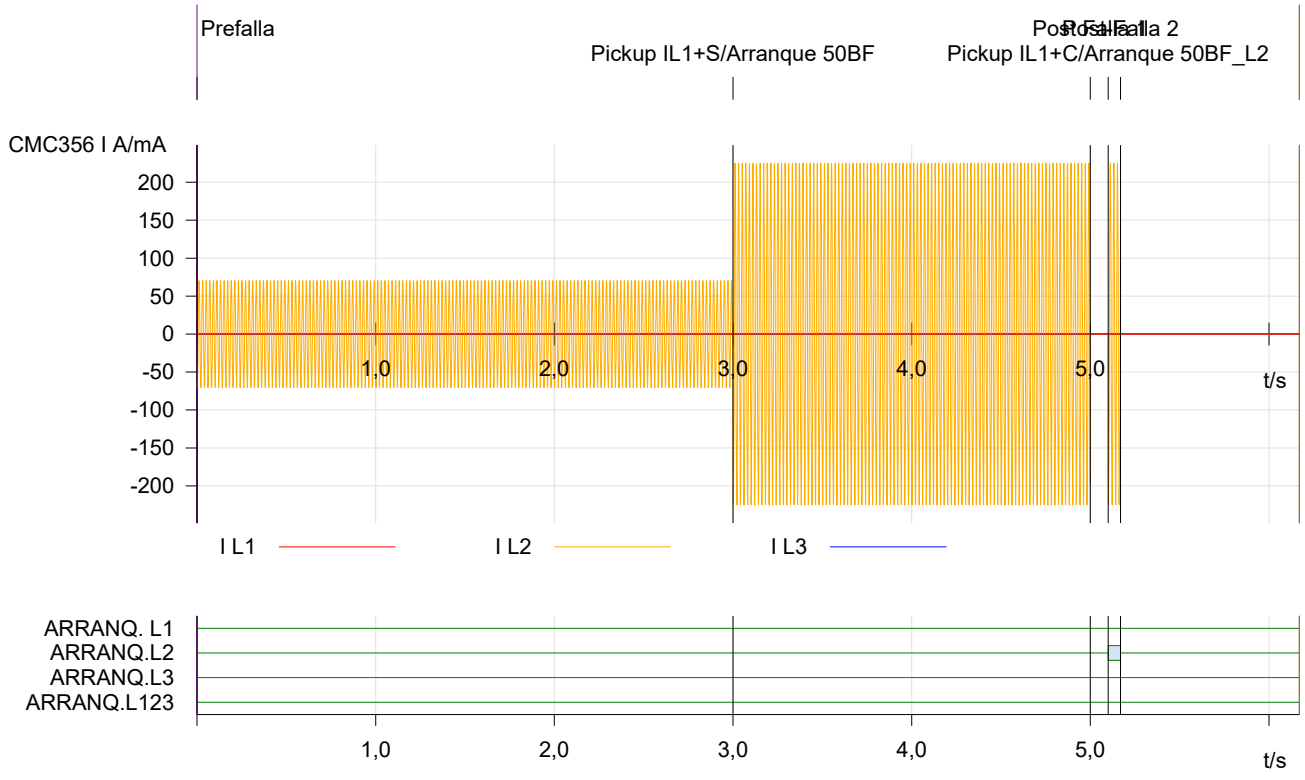
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL1+C/Arranque 50BF_L2	Pickup IL1+C/Arranque 50BF_L2	TRIP 87B-L2 0>1	50,00 ms	30,00 ms	30,00 ms	69,10 ms	19,10 ms	+

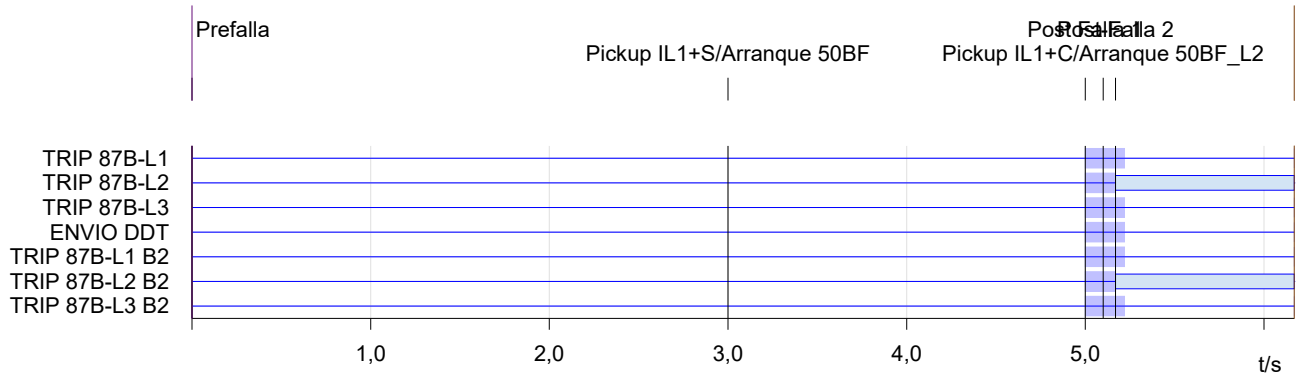
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L2	Post-Falla 2
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	50,00 ms
TRIP 87B-L1	0	0	0	0	0
TRIP 87B-L2	0	0	0	1	X
TRIP 87B-L3	0	0	0	0	0
ENVIO DDT	0	0	0	0	0
TRIP 87B-L1 B2	0	0	0	0	0
TRIP 87B-L2 B2	0	0	0	1	X
TRIP 87B-L3 B2	0	0	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	6,169 s	<none>	n/a
C2 - C1	6,169 s		n/a

Event recorder

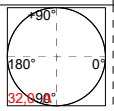
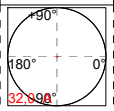
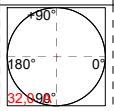
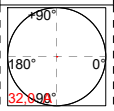
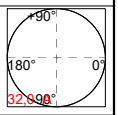
Time	Type	Signal name	Slope
5,100 s	Output	ARRANQ.L2	0>1
5,169 s	Input	TRIP 87B-L2	0>1
5,169 s	Input	TRIP 87B-L2 B2	0>1
5,169 s	Output	ARRANQ.L2	1>0
6,169 s	Input	TRIP 87B-L2	1>0
6,169 s	Input	TRIP 87B-L2 B2	1>0

Test State:
Test passed

10.3 Operacion 50BF_Fase L3:

Test Settings

State	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L3	Post-Falla 2
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	0	0
ARRANQ.L2	0	0	0	0	0
ARRANQ.L3	0	0	0	1	0
ARRANQ.L123	0	0	0	0	0
Max. State Time	3,000 s	2,000 s	1,000 s	100,0 ms	1,000 s
Trigger Logic				AND	
TRIP 87B-L3				1	
TRIP 87B-L3 B2				1	

User interaction	no	no	no	no	no
CMGPS trigger	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no
Pulses / seconds	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no
Diagrams					

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:11:52	Test End:	11-abr.-2019 01:12:01
User Name:		Manager:	
Company:			

Test Results

Time Assessment

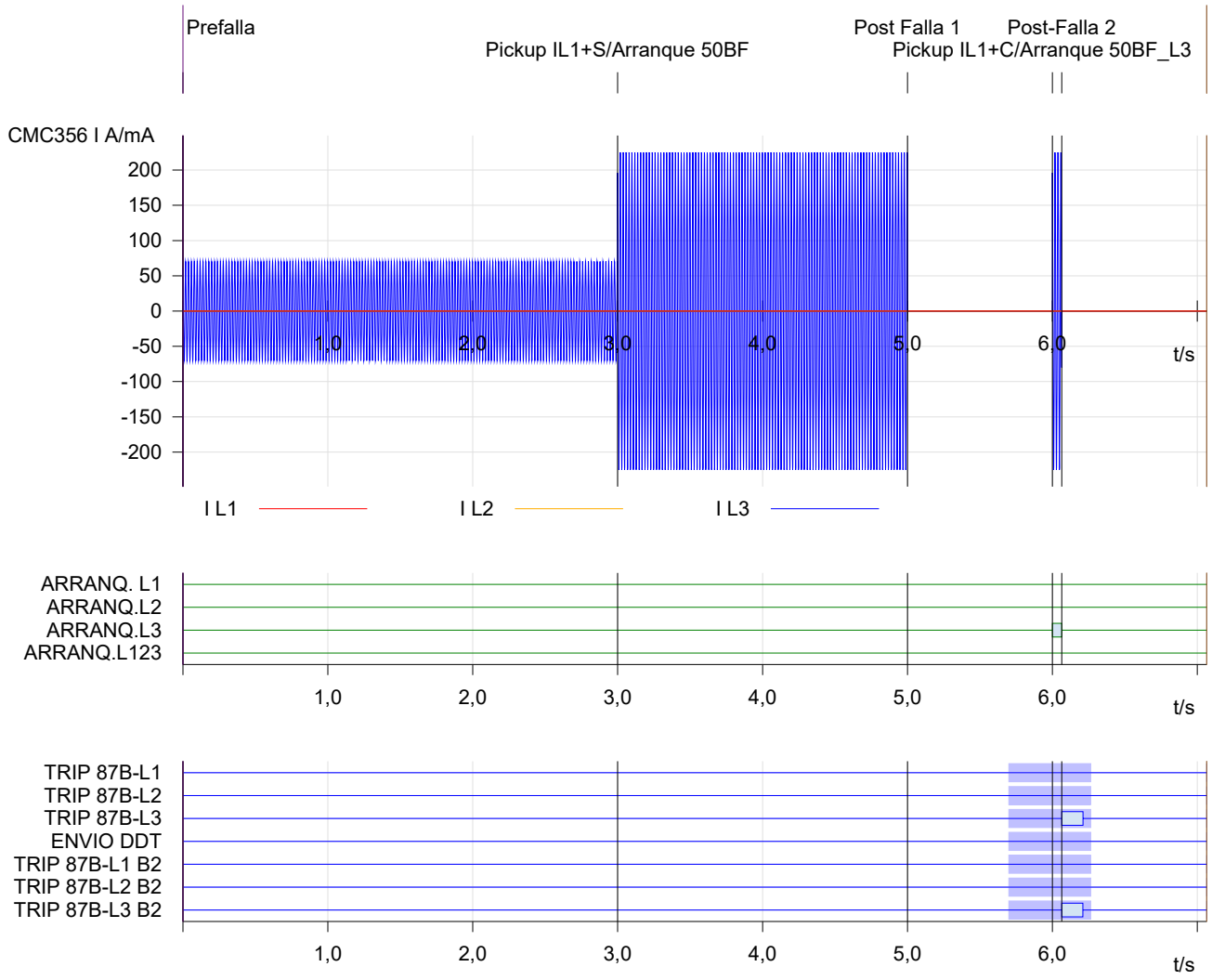
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL1+C/Arranque 50BF_L3	Pickup IL1+C/Arranque 50BF_L3	TRIP 87B-L3 0>1	50,00 ms	30,00 ms	30,00 ms	64,20 ms	14,20 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L3	Post-Falla 2
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	0	0
TRIP 87B-L2	0	0	0	0	0
TRIP 87B-L3	0	0	0	1	0
ENVIO DDT	0	0	0	0	0
TRIP 87B-L1 B2	0	0	0	0	0
TRIP 87B-L2 B2	0	0	0	0	0
TRIP 87B-L3 B2	0	0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,065 s	<none>	n/a
C2 - C1	7,065 s		n/a

Event recorder

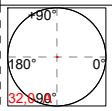
Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ.L3	0>1
6,064 s	Input	TRIP 87B-L3	0>1
6,065 s	Input	TRIP 87B-L3 B2	0>1
6,065 s	Output	ARRANQ.L3	1>0
6,211 s	Input	TRIP 87B-L3 B2	1>0
6,211 s	Input	TRIP 87B-L3	1>0

Test State:

Test passed

10.4 Operacion 50BF_Fase L123:

Test Settings

State	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L123	Post-Falla 3
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	0	0
ARRANQ.L2	0	0	0	0	0
ARRANQ.L3	0	0	0	0	0
ARRANQ.L123	0	0	0	1	0
Max. State Time	3,000 s	2,000 s	1,000 s	100,0 ms	1,000 s
Trigger Logic				AND	
TRIP 87B-L1				1	
TRIP 87B-L2				1	
TRIP 87B-L3				1	
TRIP 87B-L1 B2				1	
TRIP 87B-L2 B2				1	
TRIP 87B-L3 B2				1	
User interaction	no	no	no	no	no
CMGPS trigger	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no
Pulses / seconds	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no
Diagrams					

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:01:34	Test End:	11-abr.-2019 01:01:43
User Name:		Manager:	
Company:			

Test Results

Time Assessment

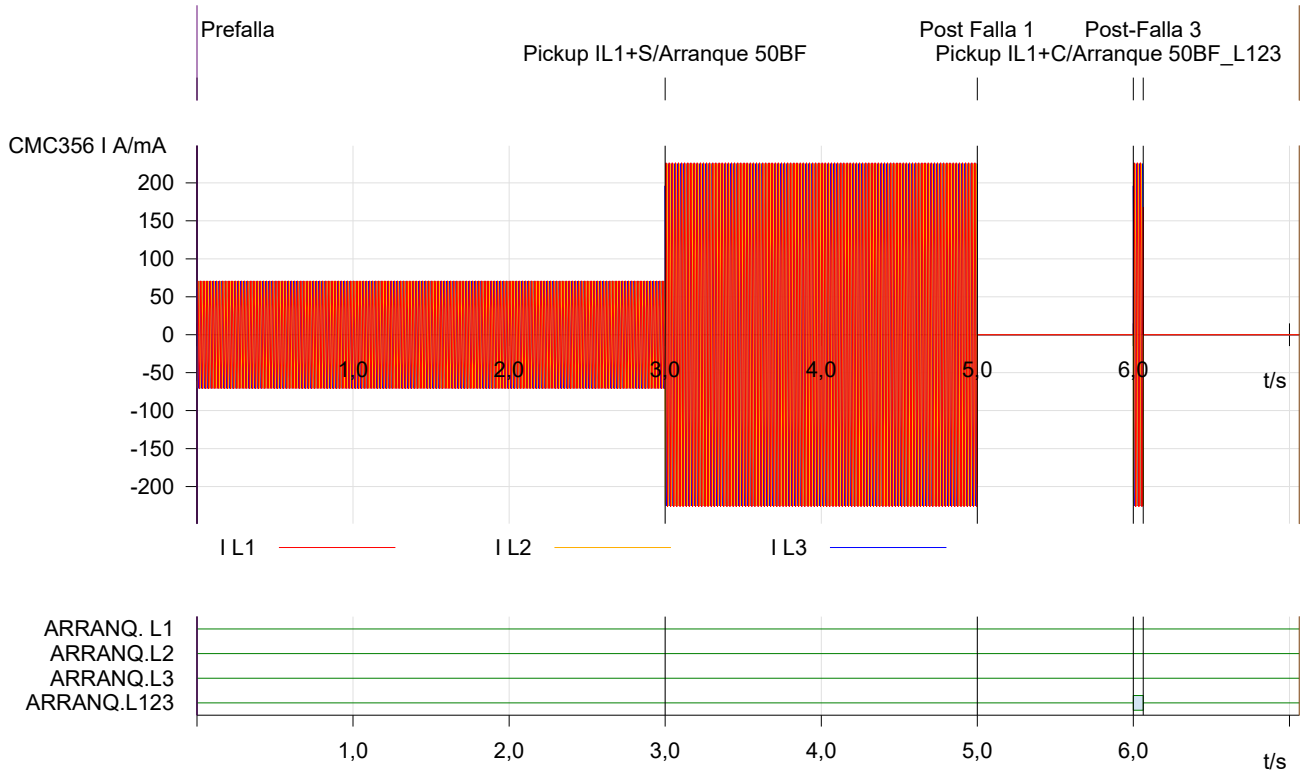
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL1+C/Arranque 50BF_L123	Pickup IL1+C/Arranque 50BF_L123	TRIP 87B-L3 0>1	50,00 ms	20,00 ms	20,00 ms	62,40 ms	12,40 ms	+

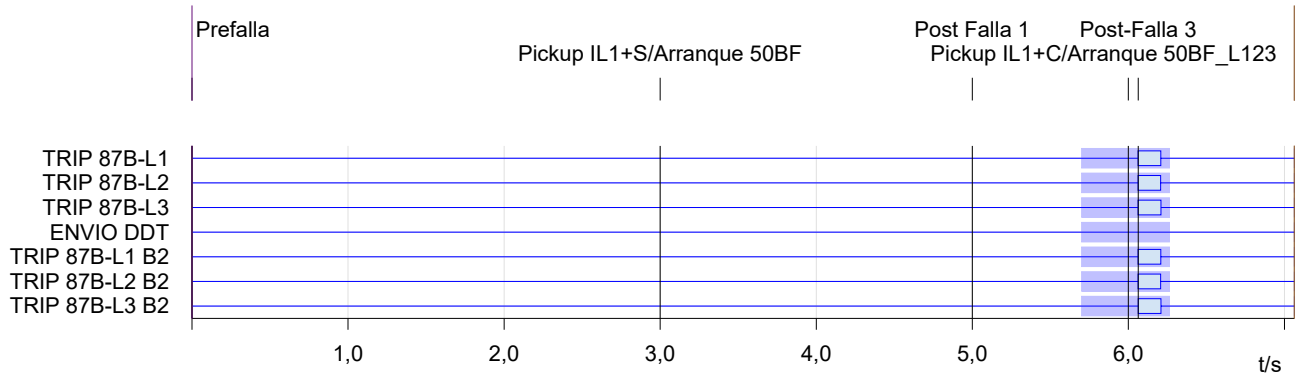
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L123	Post-Falla 3
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	1	0
TRIP 87B-L2	0	0	0	1	0
TRIP 87B-L3	0	0	0	1	0
ENVIO DDT	0	0	0	0	0
TRIP 87B-L1 B2	0	0	0	1	0
TRIP 87B-L2 B2	0	0	0	1	0
TRIP 87B-L3 B2	0	0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,063 s	<none>	n/a
C2 - C1	7,063 s		n/a

Event recorder

Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ.L123	0>1
6,062 s	Input	TRIP 87B-L2 B2	0>1
6,062 s	Input	TRIP 87B-L1	0>1
6,062 s	Input	TRIP 87B-L1 B2	0>1
6,062 s	Input	TRIP 87B-L3	0>1
6,063 s	Input	TRIP 87B-L2	0>1
6,063 s	Input	TRIP 87B-L3 B2	0>1
6,063 s	Output	ARRANQ.L123	1>0
6,207 s	Input	TRIP 87B-L2 B2	1>0
6,207 s	Input	TRIP 87B-L2	1>0
6,208 s	Input	TRIP 87B-L1	1>0
6,208 s	Input	TRIP 87B-L1 B2	1>0
6,208 s	Input	TRIP 87B-L3 B2	1>0
6,209 s	Input	TRIP 87B-L3	1>0

Test State:
Test passed

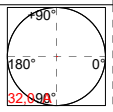
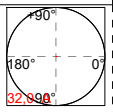
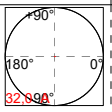
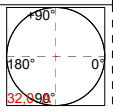
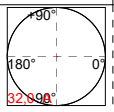
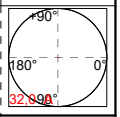
Group end:10. Operacion 50BF_J3 (T1)

Group:11. Operacion 50BF_J3 (T1 and T2)

11.1 Operacion 50BF_Fase L1 :

Test Settings

State	Prefalla	Pickup IL1+S/Arranque 50BF_L1	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	Post-Falla 2
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A	0,000 A	0,000 A	0,000 A	0,000 A	0,000 A

I L3	120,00 ° 50,000 Hz	120,00 ° 50,000 Hz	120,00 ° 50,000 Hz	120,00 ° 50,000 Hz	120,00 ° 50,000 Hz	120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	1	1	0
ARRANQ.L2	0	0	0	0	0	0
ARRANQ.L3	0	0	0	0	0	0
ARRANQ.L123	0	0	0	0	0	0
Max. State Time	3,000 s	2,000 s	1,000 s			1,000 s
Trigger Logic				AND	AND	
TRIP 87B-L1				1	X	
ENVIO DDT				X	1	
TRIP 87B-L1 B2				1	X	
User interaction	no	no	no	no	no	no
CMGPS trigger	no	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no	no
Pulses / seconds	1	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no	no
Diagrams						

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:28:19	Test End:	11-abr.-2019 01:28:28
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	TRIP 87B-L1 0>1	50,00 ms	30,00 ms	30,00 ms	66,30 ms	16,30 ms	+
Disp. 50BF_Etapa 2	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	ENVIO DDT 0>1	150,0 ms	30,00 ms	30,00 ms	176,9 ms	26,90 ms	+

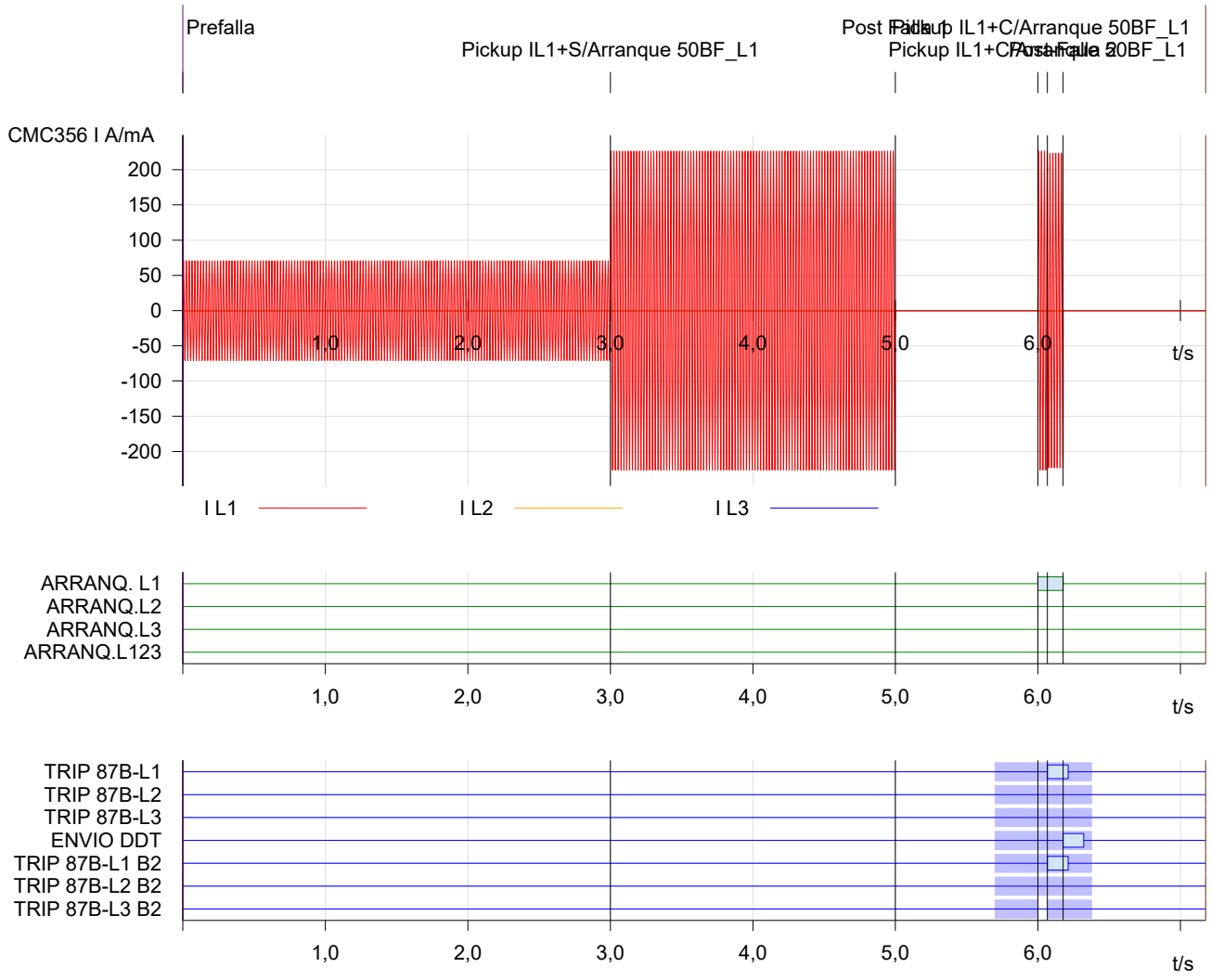
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL1+S/Arranque 50BF_L1	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	Post-Falla 2
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	500,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	1	1	0
TRIP 87B-L2	0	0	0	0	0	0
TRIP 87B-L3	0	0	0	0	0	0
ENVIO DDT	0	0	0	0	1	0
TRIP 87B-L1 B2	0	0	0	1	1	0

TRIP 87B-L2 B2	0	0	0	0	0	0
TRIP 87B-L3 B2	0	0	0	X	0	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

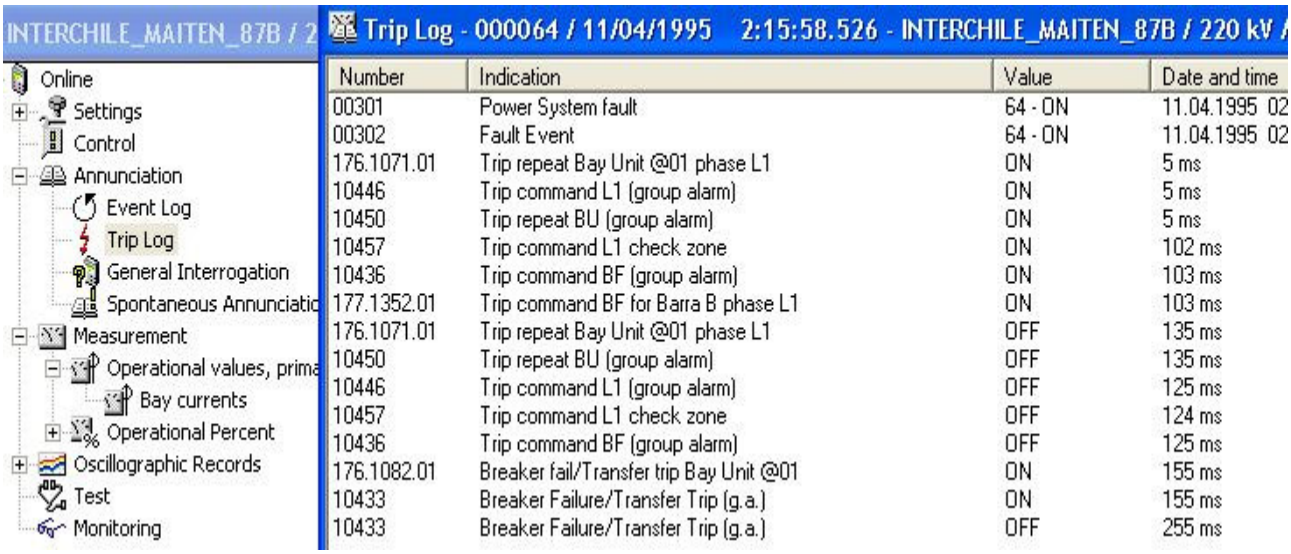
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,177 s	<none>	n/a
C2 - C1	7,177 s		n/a

Event recorder

Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ. L1	0>1
6,066 s	Input	TRIP 87B-L1	0>1
6,067 s	Input	TRIP 87B-L1 B2	0>1
6,177 s	Input	ENVIO DDT	0>1
6,177 s	Output	ARRANQ. L1	1>0
6,212 s	Input	TRIP 87B-L1	1>0
6,212 s	Input	TRIP 87B-L1 B2	1>0
6,321 s	Input	ENVIO DDT	1>0

Test State:

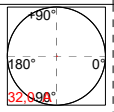
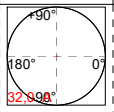
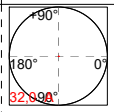
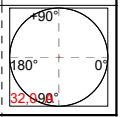
Test passed



Number	Indication	Value	Date and time
00301	Power System fault	64 - ON	11.04.1995 02
00302	Fault Event	64 - ON	11.04.1995 02
176.1071.01	Trip repeat Bay Unit @01 phase L1	ON	5 ms
10446	Trip command L1 (group alarm)	ON	5 ms
10450	Trip repeat BU (group alarm)	ON	5 ms
10457	Trip command L1 check zone	ON	102 ms
10436	Trip command BF (group alarm)	ON	103 ms
177.1352.01	Trip command BF for Barra B phase L1	ON	103 ms
176.1071.01	Trip repeat Bay Unit @01 phase L1	OFF	135 ms
10450	Trip repeat BU (group alarm)	OFF	135 ms
10446	Trip command L1 (group alarm)	OFF	125 ms
10457	Trip command L1 check zone	OFF	124 ms
10436	Trip command BF (group alarm)	OFF	125 ms
176.1082.01	Breaker fail/Transfer trip Bay Unit @01	ON	155 ms
10433	Breaker Failure/Transfer Trip (g.a.)	ON	155 ms
10433	Breaker Failure/Transfer Trip (g.a.)	OFF	255 ms

11.2 Operacion 50BF_Fase L2:

Test Settings

State	Prefalla	Pickup IL2+S/Arranque 50BF_L2	Post Falla 1	Pickup IL2+C/Arranque 50BF_L2	Pickup IL1+C/Arranque 50BF_L2	Post-Falla 2
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	300,0 mA -120,00 ° 50,000 Hz	300,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	0	0	0
ARRANQ.L2	0	0	0	1	1	0
ARRANQ.L3	0	0	0	0	0	0
ARRANQ.L123	0	0	0	0	0	0
Max. State Time	3,000 s	2,000 s	1,000 s			1,000 s
Trigger Logic				AND	AND	
TRIP 87B-L2				1	X	
ENVIO DDT				X	1	
TRIP 87B-L2 B2				1	X	
User interaction	no	no	no	no	no	no
CMGPS trigger	no	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no	no
Pulses / seconds	1	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no	no
Diagrams						

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:26:31	Test End:	11-abr.-2019 01:26:40
User Name:		Manager:	
Company:			

Test Results

Time Assessment

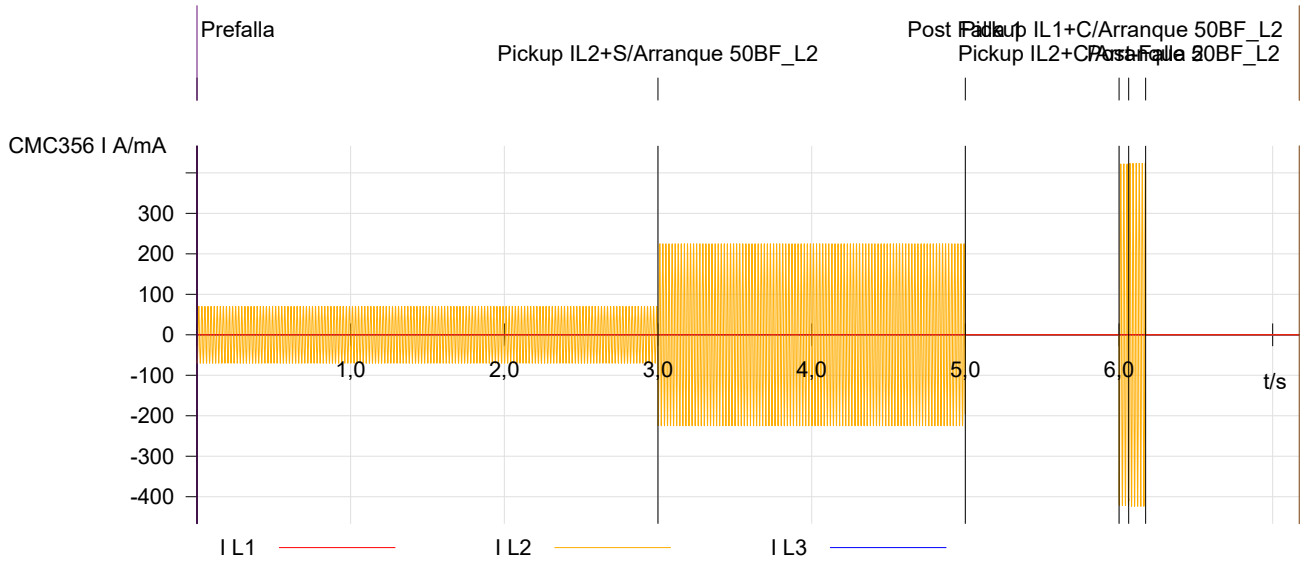
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	TRIP 87B-L2 0>1	50,00 ms	30,00 ms	30,00 ms	62,50 ms	12,50 ms	+
Disp. 50BF_Etapa 2	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	ENVIO DDT 0>1	150,0 ms	30,00 ms	30,00 ms	172,8 ms	22,80 ms	+

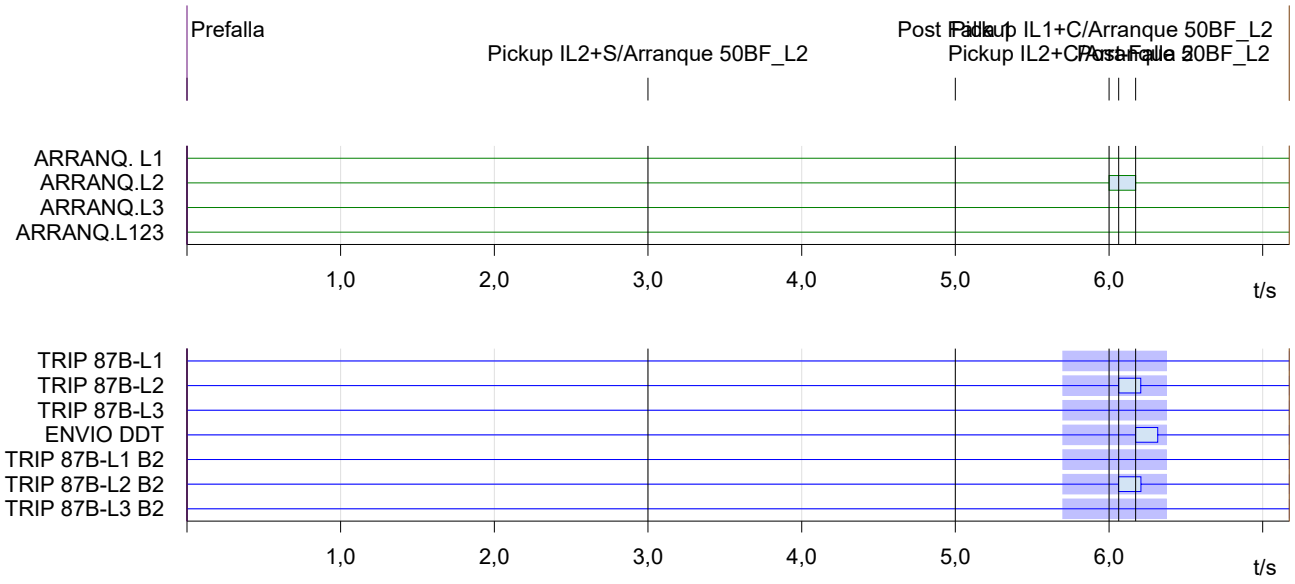
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL2+S/Arranque 50BF_L2	Post Falla 1	Pickup IL2+C/Arranque 50BF_L2	Pickup IL1+C/Arranque 50BF_L2	Post-Falla 2
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	300,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	0	0	0
TRIP 87B-L2	0	0	0	1	0	0
TRIP 87B-L3	0	0	0	0	0	0
ENVIO DDT	0	0	0	0	1	0
TRIP 87B-L1 B2	0	0	0	0	0	0
TRIP 87B-L2 B2	0	0	0	1	0	0
TRIP 87B-L3 B2	0	0	0	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed





Cursor Data

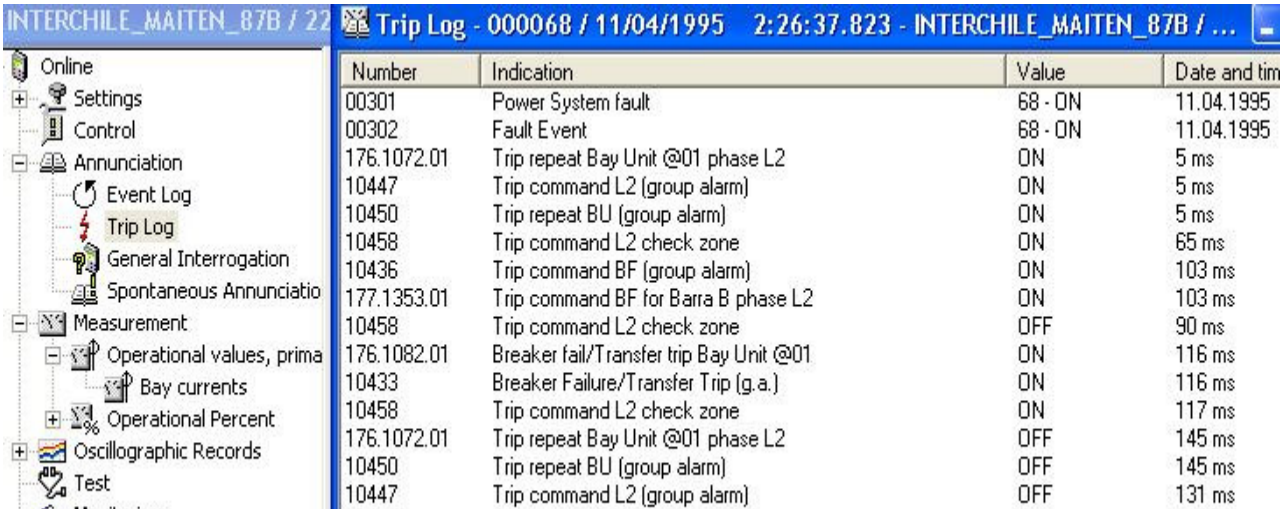
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,173 s	<none>	n/a
C2 - C1	7,173 s		n/a

Event recorder

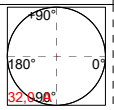
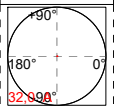
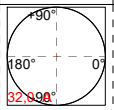
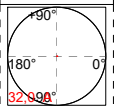
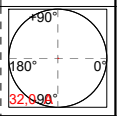
Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ.L2	0>1
6,062 s	Input	TRIP 87B-L2 B2	0>1
6,063 s	Input	TRIP 87B-L2	0>1
6,173 s	Input	ENVIO DDT	0>1
6,173 s	Output	ARRANQ.L2	1>0
6,207 s	Input	TRIP 87B-L2	1>0
6,207 s	Input	TRIP 87B-L2 B2	1>0
6,317 s	Input	ENVIO DDT	1>0

Test State:

Test passed



Test Settings

State	Prefalla	Pickup IL2+S/Arranque 50BF_L3	Post Falla 1	Pickup IL2+C/Arranque 50BF_L3	Pickup IL1+C/Arranque 50BF_L3	Post-Falla 3
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	300,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	0	0	0
ARRANQ.L2	0	0	0	0	0	0
ARRANQ.L3	0	0	0	1	1	0
ARRANQ.L123	0	0	0	0	0	0
Max. State Time	3,000 s	2,000 s	1,000 s			1,000 s
Trigger Logic				AND	AND	
TRIP 87B-L3				1	X	
ENVIO DDT				X	1	
TRIP 87B-L3 B2				1	X	
User interaction	no	no	no	no	no	no
CMGPS trigger	no	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no	no
Pulses / seconds	1	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no	no
Diagrams						

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:31:02	Test End:	11-abr.-2019 01:31:11
User Name:		Manager:	
Company:			

Test Results

Time Assessment

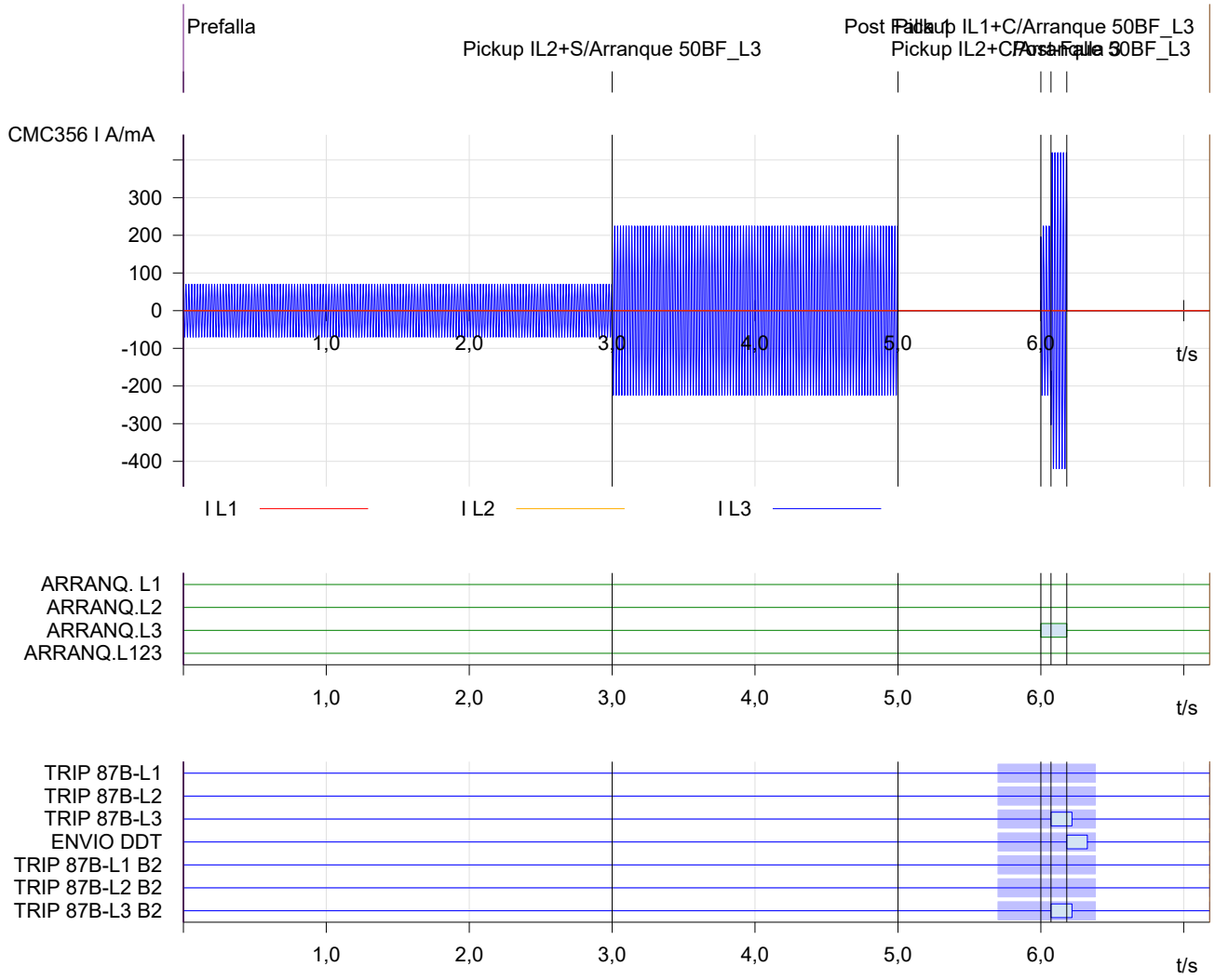
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL2+C/Arranque 50BF_L3	Pickup IL2+C/Arranque 50BF_L3	TRIP 87B-L3 0>1	50,00 ms	30,00 ms	30,00 ms	70,50 ms	20,50 ms	+
Disp. 50BF_Etapa 2	Pickup IL2+C/Arranque 50BF_L3	Pickup IL2+C/Arranque 50BF_L3	ENVIO DDT 0>1	200,0 ms	30,00 ms	30,00 ms	181,0 ms	-19,00 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL2+S/Arranque 50BF_L3	Post Falla 1	Pickup IL2+C/Arranque 50BF_L3	Pickup IL1+C/Arranque 50BF_L3	Post-Falla 3
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	300,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	0	0	0
TRIP 87B-L2	0	0	0	0	0	0
TRIP 87B-L3	0	0	0	1	0	0
ENVIO DDT	0	0	0	0	1	0
TRIP 87B-L1 B2	0	0	0	0	0	0
TRIP 87B-L2 B2	0	0	0	0	0	0
TRIP 87B-L3 B2	0	0	0	1	0	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

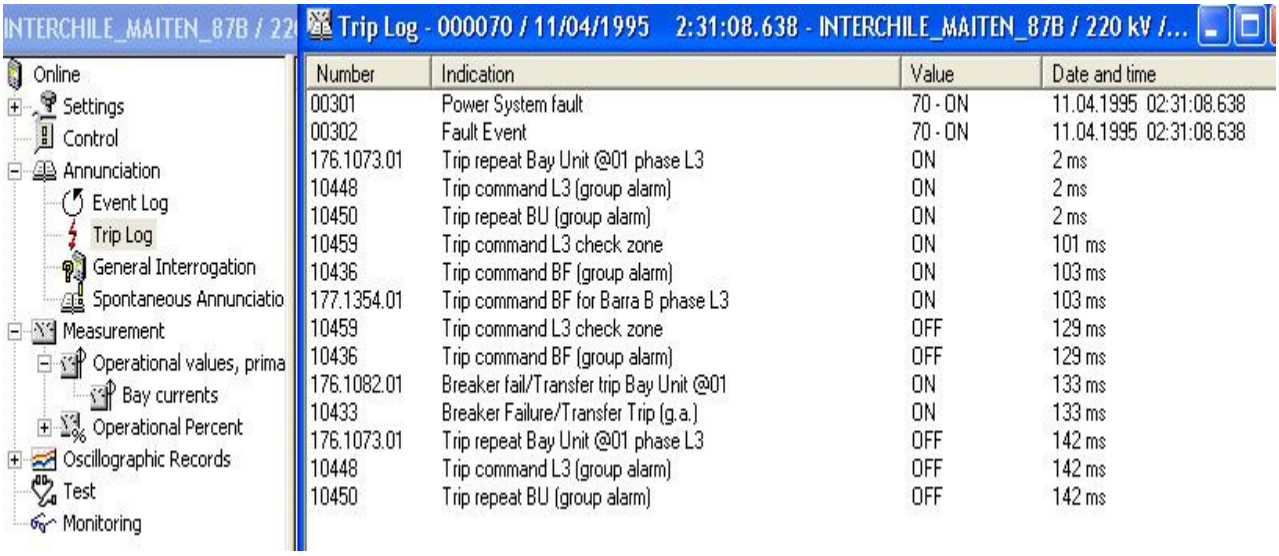
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,181 s	<none>	n/a
C2 - C1	7,181 s		n/a

Event recorder

Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ.L3	0>1
6,071 s	Input	TRIP 87B-L3	0>1
6,071 s	Input	TRIP 87B-L3 B2	0>1
6,181 s	Input	ENVIO DDT	0>1
6,181 s	Output	ARRANQ.L3	1>0
6,218 s	Input	TRIP 87B-L3 B2	1>0
6,218 s	Input	TRIP 87B-L3	1>0
6,325 s	Input	ENVIO DDT	1>0

Test State:

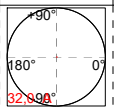
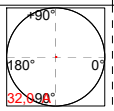
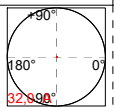
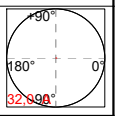
Test passed



11.4 Operacion 50BF_Fase L123:

Test Settings

State	Prefalla	Pickup IL2+S/Arranque 50BF_L123	Post Falla 1	Pickup IL2+C/Arranque 50BF_L123	Pickup IL1+C/Arranque 50BF_L123	Post-Falla 3
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
ARRANQ. L1	0	0	0	0	0	0
ARRANQ.L2	0	0	0	0	0	0
ARRANQ.L3	0	0	0	0	0	0
ARRANQ.L123	0	0	0	1	1	0
Max. State Time	3,000 s	2,000 s	1,000 s			1,000 s
Trigger Logic				AND	AND	
TRIP 87B-L1				1	X	

TRIP 87B-L2				1	X	
TRIP 87B-L3				1	X	
ENVIO DDT				X	1	
TRIP 87B-L1 B2				1	1	
TRIP 87B-L2 B2				1	X	
TRIP 87B-L3 B2				1	X	
User interaction	no	no	no	no	no	no
CMGPS trigger	no	no	no	no	no	no
IRIG-B/PTP trigger	no	no	no	no	no	no
Pulses / seconds	1	1	1	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no	no	no	no
Diagrams						

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:34:29	Test End:	11-abr.-2019 01:34:38
User Name:		Manager:	
Company:			

Test Results

Time Assessment

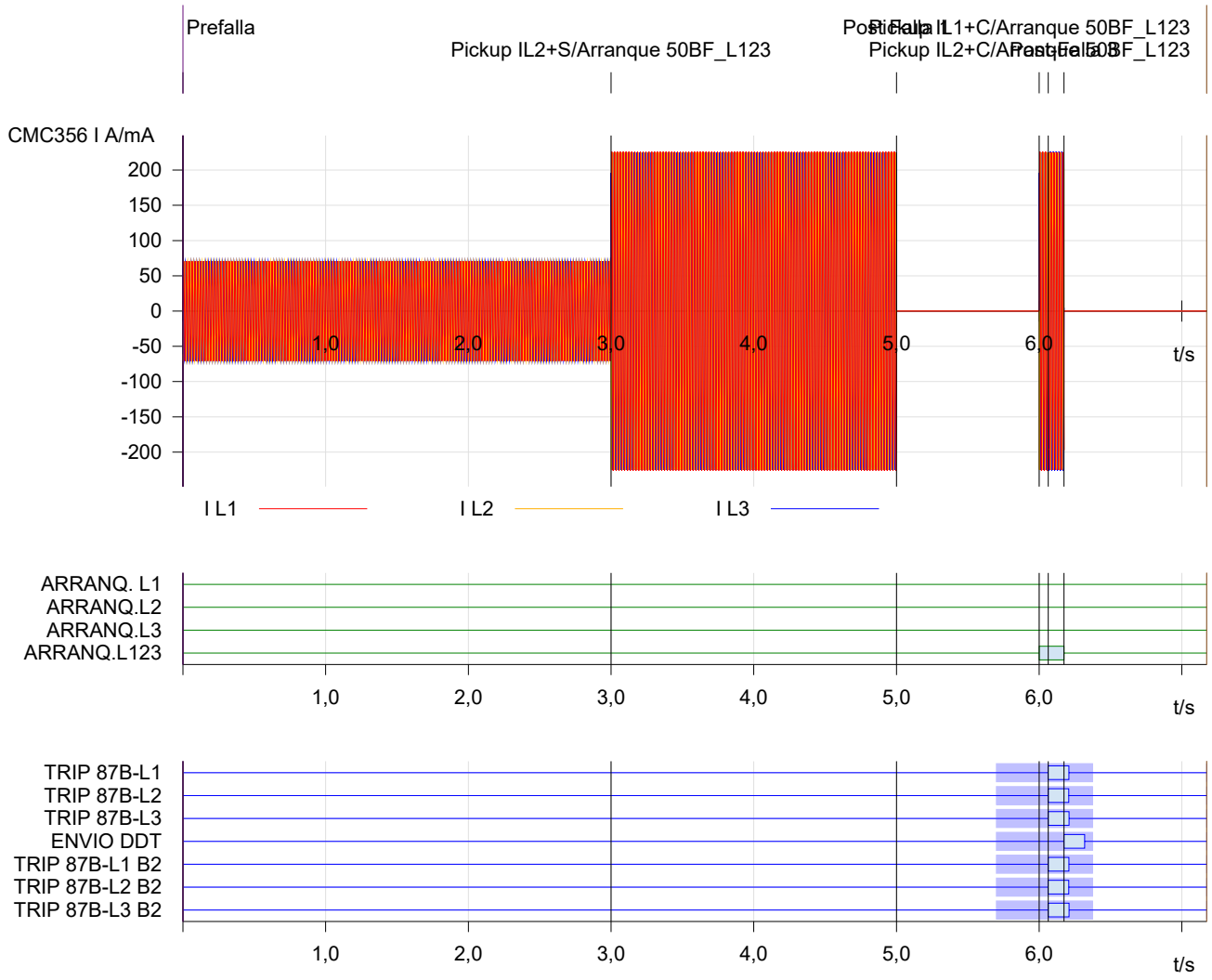
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL2+C/Arranque 50BF_L123	Pickup IL2+C/Arranque 50BF_L123	TRIP 87B-L3 B2 0>1	50,00 ms	30,00 ms	30,00 ms	63,30 ms	13,30 ms	+
Disp. 50BF_Etapa 2	Pickup IL2+C/Arranque 50BF_L123	Pickup IL2+C/Arranque 50BF_L123	ENVIO DDT 0>1	200,0 ms	30,00 ms	30,00 ms	173,4 ms	-26,60 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL2+S/Arranque 50BF_L123	Post Falla 1	Pickup IL2+C/Arranque 50BF_L123	Pickup IL1+C/Arranque 50BF_L123	Post-Falla 3
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	300,0 ms	200,0 ms
TRIP 87B-L1	0	0	0	1	0	0
TRIP 87B-L2	0	0	0	1	0	0
TRIP 87B-L3	0	0	0	1	0	0
ENVIO DDT	0	0	0	0	1	0
TRIP 87B-L1 B2	0	0	0	1	0	0
TRIP 87B-L2 B2	0	0	0	1	0	0
TRIP 87B-L3 B2	0	0	0	1	0	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

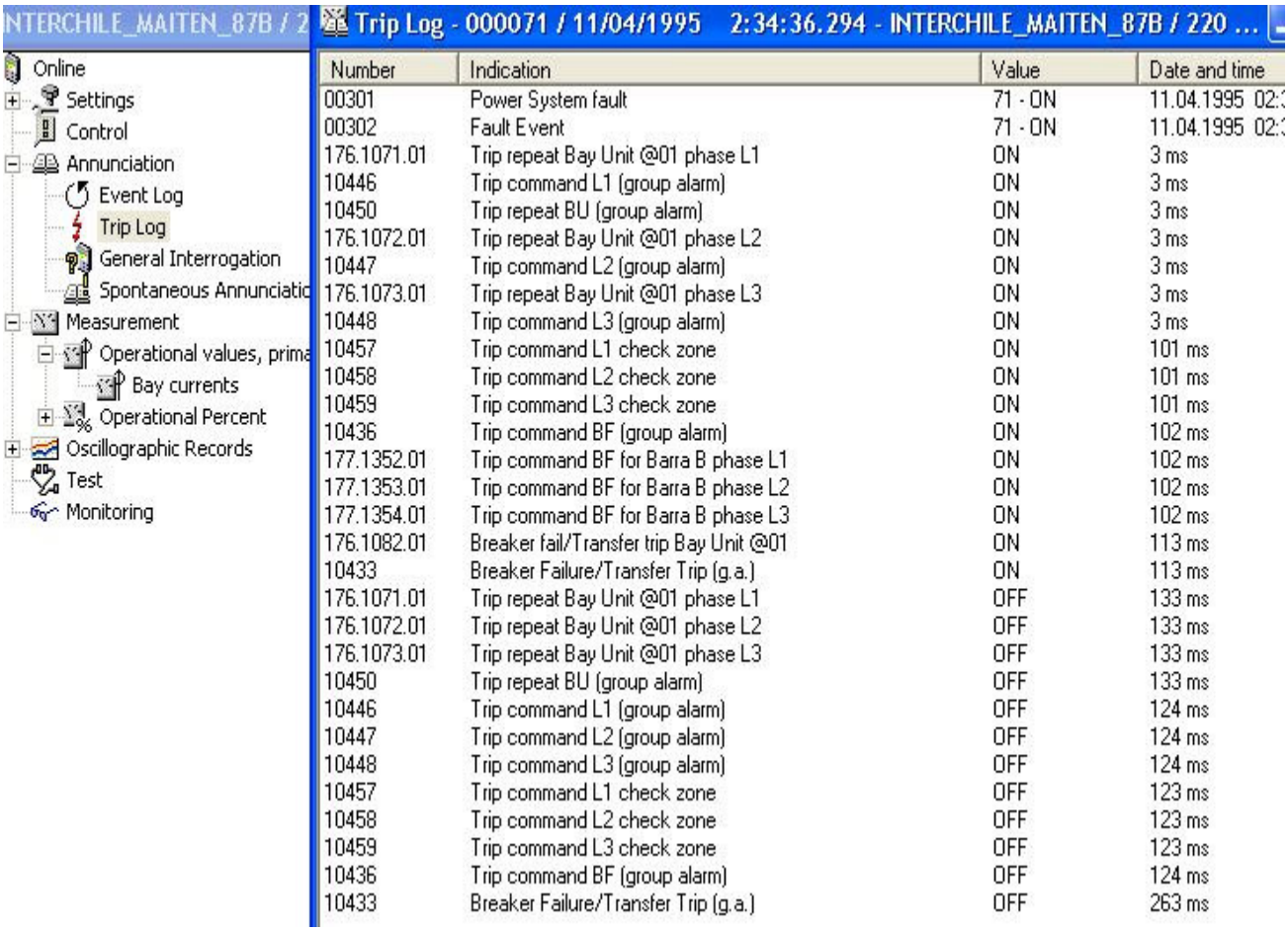
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	7,173 s	<none>	n/a
C2 - C1	7,173 s		n/a

Event recorder

Time	Type	Signal name	Slope
6,000 s	Output	ARRANQ.L123	0>1
6,063 s	Input	TRIP 87B-L2 B2	0>1
6,063 s	Input	TRIP 87B-L1	0>1
6,063 s	Input	TRIP 87B-L3	0>1
6,063 s	Input	TRIP 87B-L1 B2	0>1
6,063 s	Input	TRIP 87B-L2	0>1
6,063 s	Input	TRIP 87B-L3 B2	0>1
6,173 s	Input	ENVIO DDT	0>1
6,173 s	Output	ARRANQ.L123	1>0
6,208 s	Input	TRIP 87B-L2	1>0
6,208 s	Input	TRIP 87B-L2 B2	1>0
6,208 s	Input	TRIP 87B-L1 B2	1>0
6,209 s	Input	TRIP 87B-L1	1>0
6,209 s	Input	TRIP 87B-L3 B2	1>0

6,210 s	Input	TRIP 87B-L3	1>0
6,318 s	Input	ENVIO DDT	1>0

Test State:
Test passed



Number	Indication	Value	Date and time
00301	Power System fault	71 - ON	11.04.1995 02:
00302	Fault Event	71 - ON	11.04.1995 02:
176.1071.01	Trip repeat Bay Unit @01 phase L1	ON	3 ms
10446	Trip command L1 (group alarm)	ON	3 ms
10450	Trip repeat BU (group alarm)	ON	3 ms
176.1072.01	Trip repeat Bay Unit @01 phase L2	ON	3 ms
10447	Trip command L2 (group alarm)	ON	3 ms
176.1073.01	Trip repeat Bay Unit @01 phase L3	ON	3 ms
10448	Trip command L3 (group alarm)	ON	3 ms
10457	Trip command L1 check zone	ON	101 ms
10458	Trip command L2 check zone	ON	101 ms
10459	Trip command L3 check zone	ON	101 ms
10436	Trip command BF (group alarm)	ON	102 ms
177.1352.01	Trip command BF for Barra B phase L1	ON	102 ms
177.1353.01	Trip command BF for Barra B phase L2	ON	102 ms
177.1354.01	Trip command BF for Barra B phase L3	ON	102 ms
176.1082.01	Breaker fail/Transfer trip Bay Unit @01	ON	113 ms
10433	Breaker Failure/Transfer Trip (g.a.)	ON	113 ms
176.1071.01	Trip repeat Bay Unit @01 phase L1	OFF	133 ms
176.1072.01	Trip repeat Bay Unit @01 phase L2	OFF	133 ms
176.1073.01	Trip repeat Bay Unit @01 phase L3	OFF	133 ms
10450	Trip repeat BU (group alarm)	OFF	133 ms
10446	Trip command L1 (group alarm)	OFF	124 ms
10447	Trip command L2 (group alarm)	OFF	124 ms
10448	Trip command L3 (group alarm)	OFF	124 ms
10457	Trip command L1 check zone	OFF	123 ms
10458	Trip command L2 check zone	OFF	123 ms
10459	Trip command L3 check zone	OFF	123 ms
10436	Trip command BF (group alarm)	OFF	124 ms
10433	Breaker Failure/Transfer Trip (g.a.)	OFF	263 ms

----------Group end:11. Operacion 50BF_J3 (T1 and T2)----------
----------Group:12. Operacion End Fault_50BF E0----------

Hardware

Test Equipment

Type	Serial Number
CMC356	MC355V

Hardware Check

Performed At	Result	Details
11-04-2019 1:42:19	Passed	

Analog Outputs

Test Equipment		Test Object		
Device	**Connector**	**Display Name**	**Connection Terminal**	
CMC356 I A MC355V	1 2 3 N	I L1 I L2 I L3		

Binary/Analog Inputs

Test Equipment		Test Object		
Device	**Connector**	**Display Name**	**Connection Terminal**	
CMC356 MC355V	1+ 1- 2+ 2- 3+ 3- 4+ 4- 5+ 5- 6+ 6- 7+ 7- 8+ 8- 9+ 9- 10+ 10- 1 2 N	Disp.L1_52J2 Disp.L2_52J2 Disp.L3_52J2 DDT Etapa 0 50BF ET0 Bin. in 6 Bin. in 7 Bin. in 8 Bin. in 9 Bin. in 10 Bin. in 11 Bin. in 12		

Binary Outputs

Test Equipment		Test Object		
Device	**Connector**	**Display Name**	**Connection Terminal**	
CMC356 MC355V	1+ 1- 2+ 2- 3+ 3- 4+ 4- 11 12 13 14 N	52J3_Open 52J3_Close Bin. out 3 Bin. out 4 Bin. out 5 Bin. out 6 Bin. out 7 Bin. out 8		

Analog DC Inputs

Test Equipment		Test Object		
Device	**Connector**	**Display Name**	**Connection Terminal**	

Group:12.1 Verificacion Pickup_End Fault

12.1.1 Pickup con Arranque Fase L1:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52K2_Open	1
52K2_Close	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52J2	X
Disp.L2_52J2	X
Disp.L3_52J2	X
DDT Etapa 0	1
50BF ET0	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 01:47:55
Test End: 11-abr.-2019 01:48:02
User Name:
Manager:
Company:

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	DDT Etapa 0 0->1 and 50BF ET0 0->1	I L1	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	46,00 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

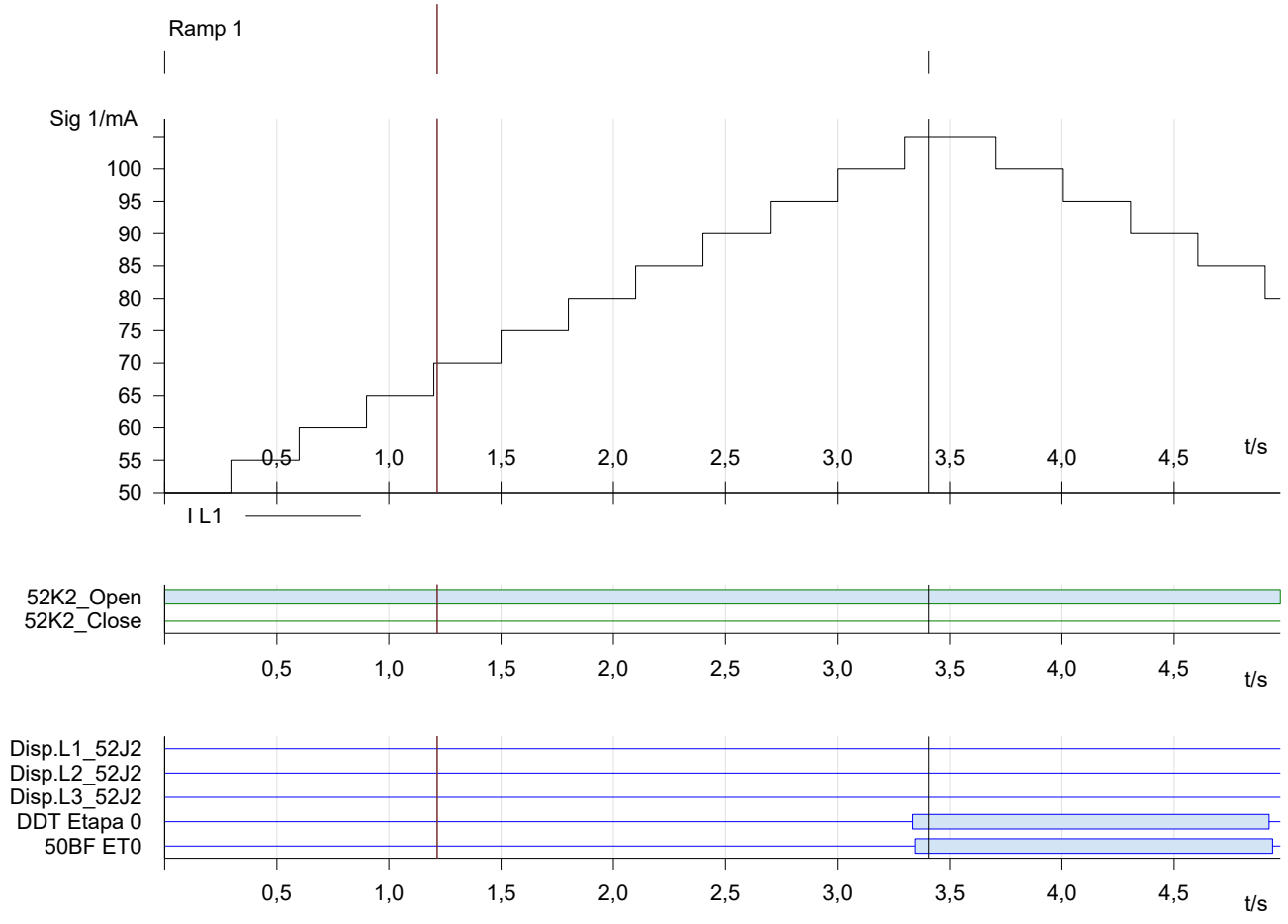
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value

Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:
Test passed

12.1.2 Pickup con Arranque Fase L2:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J3_Open	1
52J3_Close	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52J2	X
Disp.L2_52J2	X
Disp.L3_52J2	X
DDT Etapa 0	1
50BF ET0	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 01:50:20
Test End: 11-abr.-2019 01:50:27
User Name:
Manager:
Company:

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	50BF ET0 0->1 and DDT Etapa 0 0->1	I L2	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	31,10 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

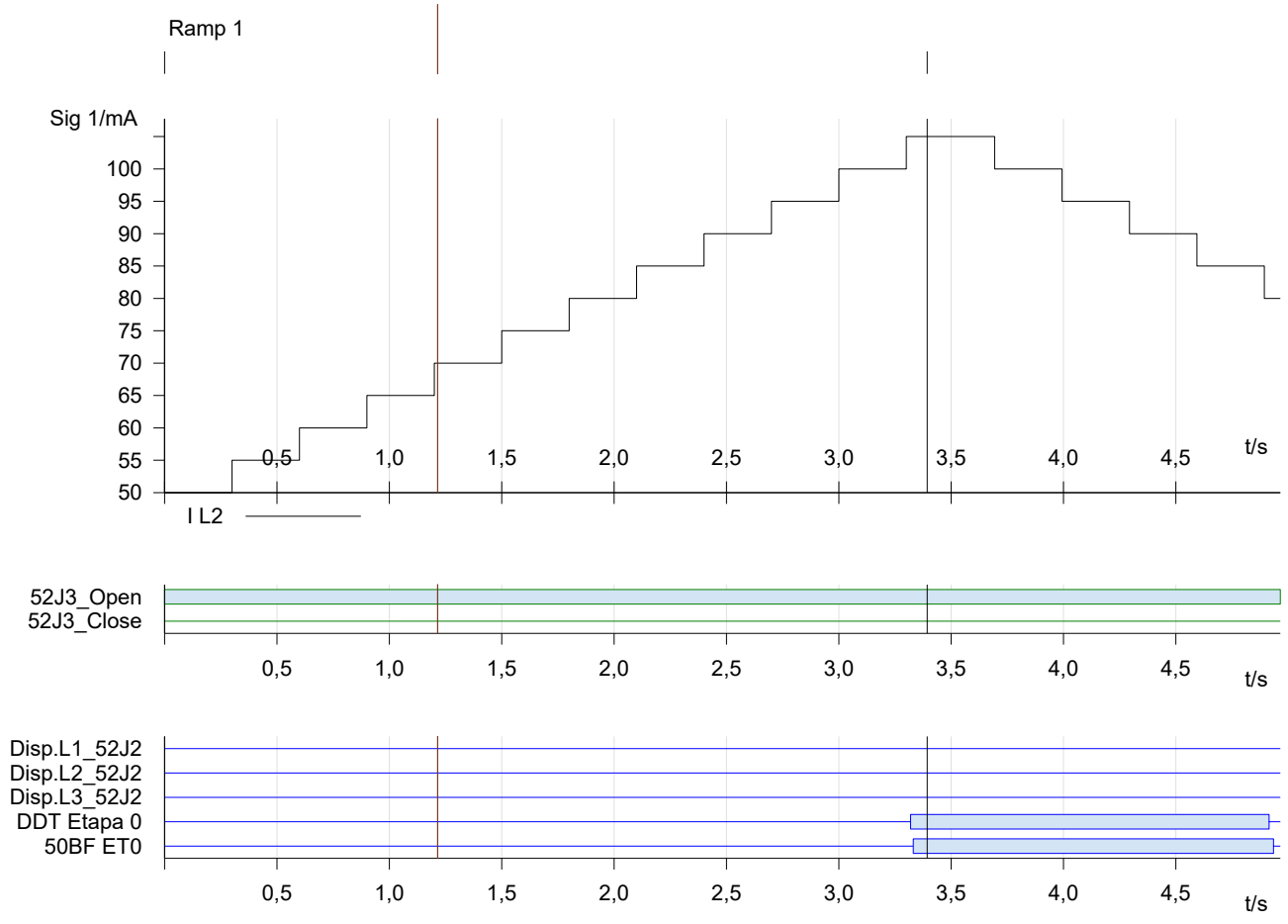
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value

Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:
Test passed

12.1.3 Pickup con Arranque Fase L3:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J3_Open	1
52J3_Close	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52J2	X
Disp.L2_52J2	X
Disp.L3_52J2	X
DDT Etapa 0	1
50BF ET0	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 01:51:04
Test End: 11-abr.-2019 01:51:11
User Name:
Manager:
Company:

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	50BF ET0 0->1 and DDT Etapa 0 0->1	I L3	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	48,90 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

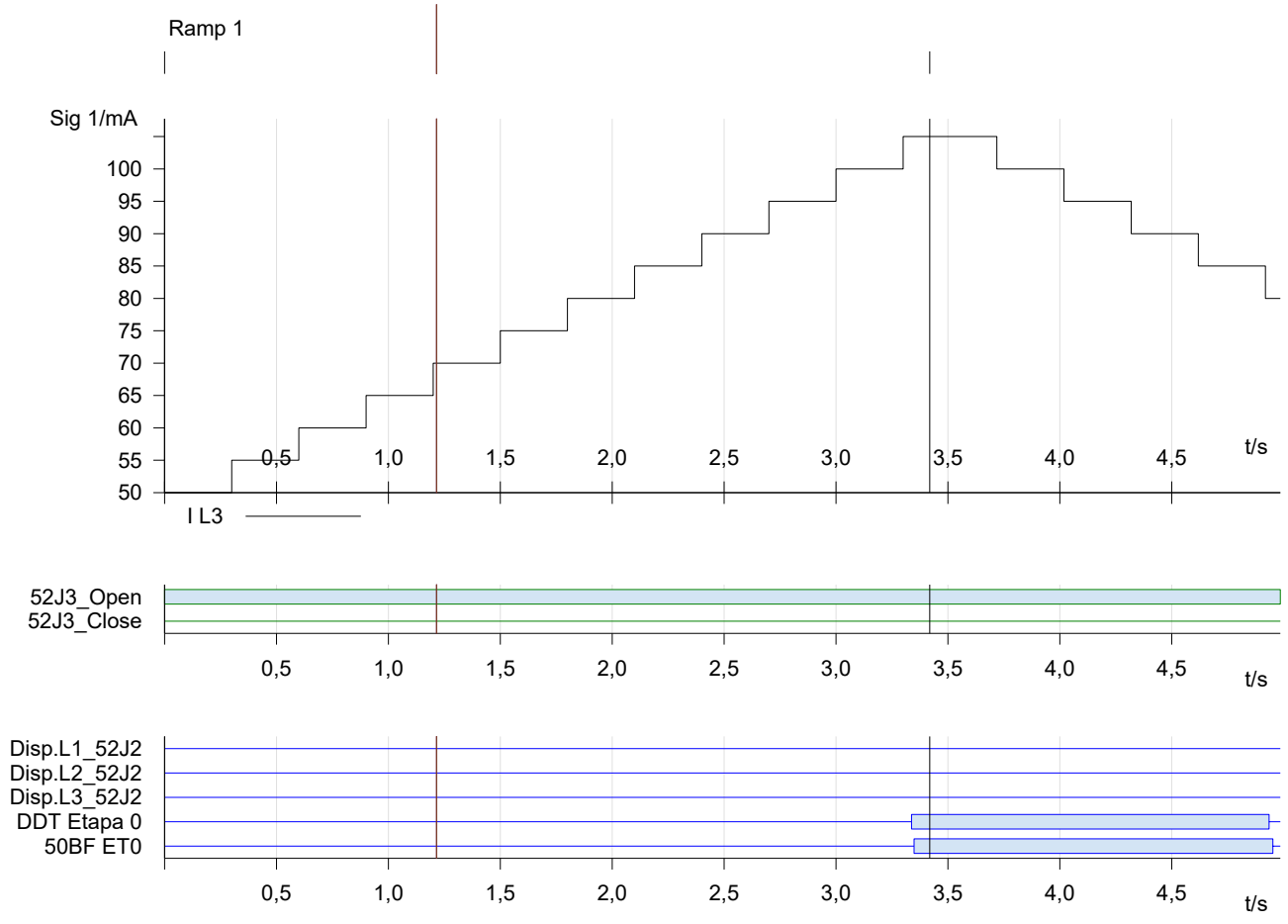
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value

Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:
Test passed

12.1.4 Pickup con Arranque Fase L123:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J3_Open	1
52J3_Close	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52J2	X
Disp.L2_52J2	X
Disp.L3_52J2	X
DDT Etapa 0	1
50BF ET0	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 01:51:47
Test End: 11-abr.-2019 01:51:54
User Name:
Manager:
Company:

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	50BF ET0 0->1 and DDT Etapa 0 0->1	I L1; L2; L3	100,0 mA	105,0 mA	20,00 mA	20,00 mA	5,000 mA	+	37,20 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

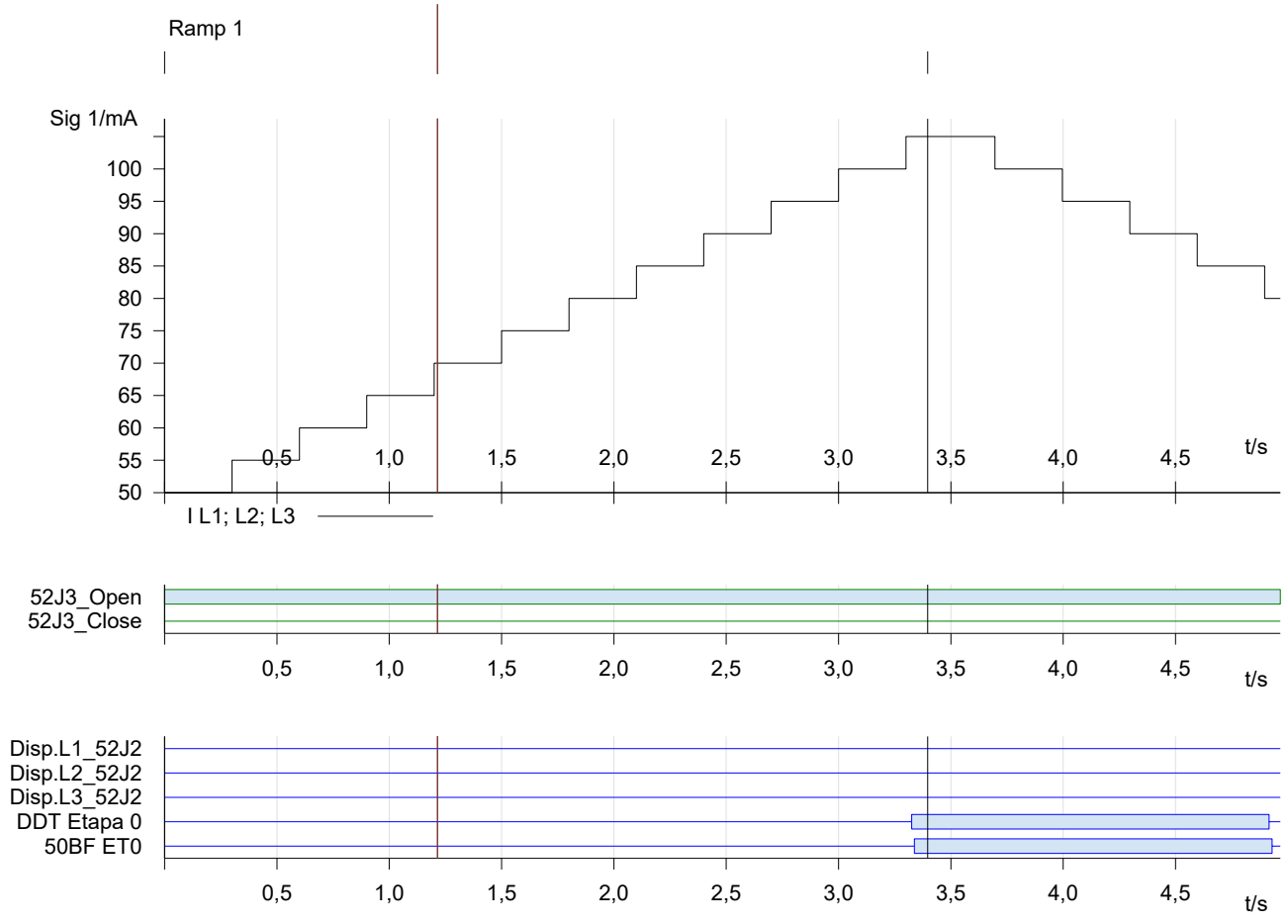
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value

Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:
Test passed

12.1.5 Pickup sin Arranque Fase L123:

Test Settings

General

No. of ramp states: 1
Total steps per test: 23
Total time per test: 6,900 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	50,00 mA 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	50,00 mA
Sig 1 To	160,0 mA
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J3_Open	0
52J3_Close	0
dt per Step	300,0 ms
Ramp Steps	23
Ramp Time	6,900s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52J2	X
Disp.L2_52J2	X
Disp.L3_52J2	X
DDT Etapa 0	1
50BF ET0	1
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 02:01:10
Test End: 11-abr.-2019 02:01:19
User Name:
Manager:
Company:

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Results

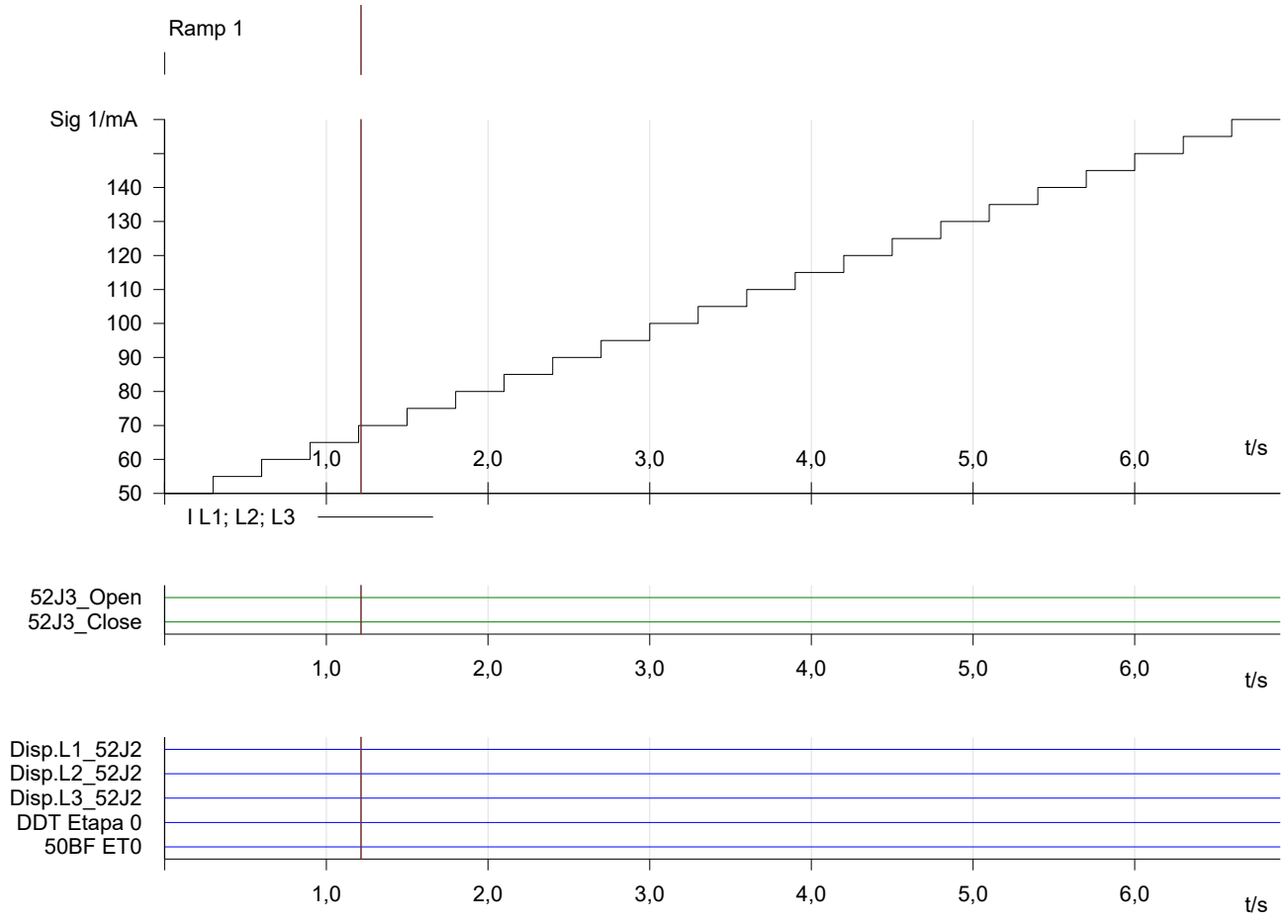
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	1,215 s	<none>	n/a
Cursor 2	1,215 s	<none>	n/a
C2 - C1	0,000 s		n/a

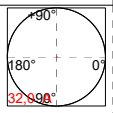
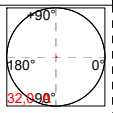
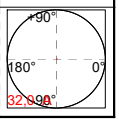
Test State:
Test passed

Group end:12.1 Verificacion Pickup_End Fault

Group:12.2 Operacion End Fault

12.2.1 Operacion End Fault_L1:

Test Settings

State	Prefalla	Falla L1+52J3 Open	Post Falla
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
52J3_Open	1	1	0
52J3_Close	0	0	0
Max. State Time	3,000 s	100,0 ms	2,000 s
Trigger Logic		AND	
50BF ET0		1	
User interaction	no	no	no
CMGPS trigger	no	no	no
IRIG-B/PTP trigger	no	no	no
Pulses / seconds	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no
Diagrams			

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:56:46	Test End:	11-abr.-2019 01:56:52
User Name:		Manager:	
Company:			

Test Results

Time Assessment

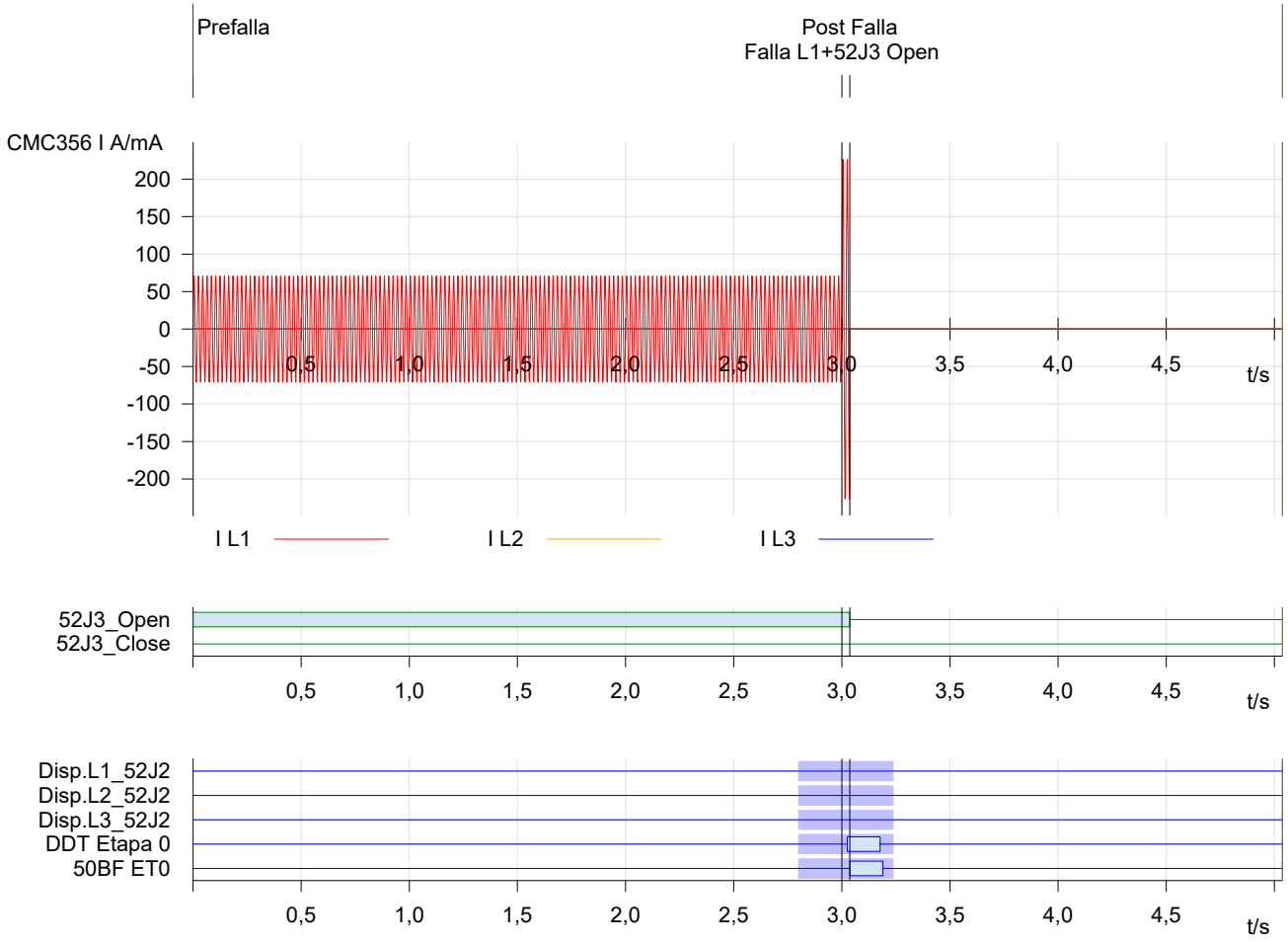
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L1+52J3 Open	Falla L1+52J3 Open	50BF ET0 0>1	50,00 ms	30,00 ms	30,00 ms	36,50 ms	-13,50 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L1+52J3 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms
Disp.L1_52J2	0	0	0
Disp.L2_52J2	0	0	0
Disp.L3_52J2	0	0	0
DDT Etapa 0	0	0	0
50BF ET0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	5,037 s	<none>	n/a
C2 - C1	5,037 s		n/a

Event recorder

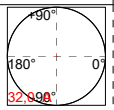
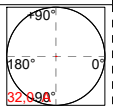
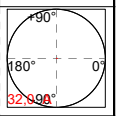
Time	Type	Signal name	Slope
3,025 s	Input	DDT Etapa 0	0>1
3,037 s	Input	50BF ET0	0>1

3,037 s	Output	52J3_Open	1>0
3,177 s	Input	DDT Etapa 0	1>0
3,189 s	Input	50BF ET0	1>0

Test State:
Test passed

12.2.2 Operacion End Fault_L2:

Test Settings

State	Prefalla	Falla L2+52J3 Open	Post Falla
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
52J3_Open	1	1	0
52J3_Close	0	0	0
Max. State Time	3,000 s	100,0 ms	2,000 s
Trigger Logic		AND	
50BF ET0		1	
User interaction	no	no	no
CMGPS trigger	no	no	no
IRIG-B/PTP trigger	no	no	no
Pulses / seconds	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no
Diagrams			

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:57:11	Test End:	11-abr.-2019 01:57:18
User Name:		Manager:	
Company:			

Test Results

Time Assessment

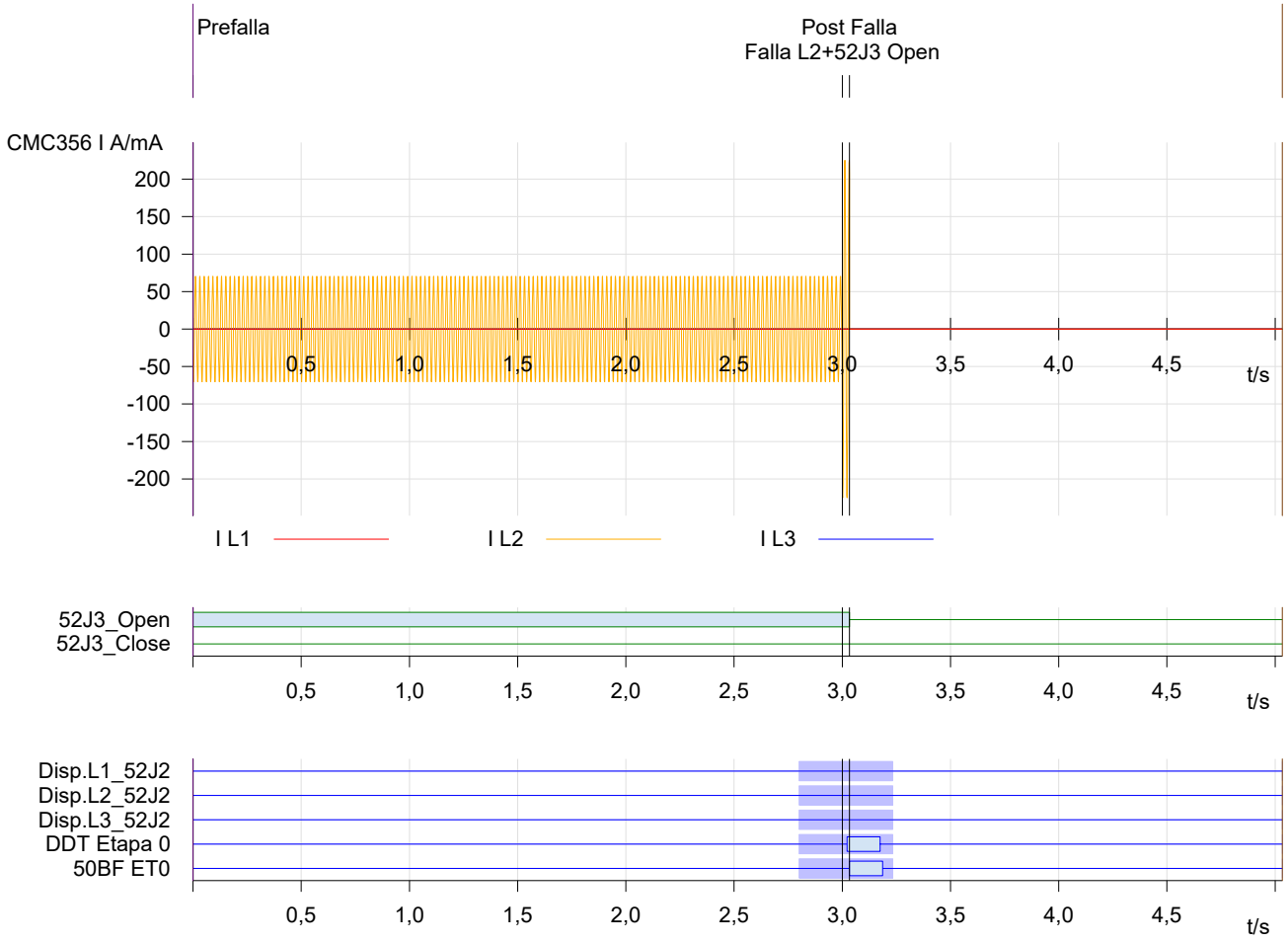
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L2+52J3 Open	Falla L2+52J3 Open	50BF ET0 0>1	50,00 ms	30,00 ms	30,00 ms	33,00 ms	-17,00 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L2+52J3 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms
Disp.L1_52J2	0	0	0
Disp.L2_52J2	0	0	0
Disp.L3_52J2	0	0	0
DDT Etapa 0	0	1	0
50BF ET0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	5,033 s	<none>	n/a
C2 - C1	5,033 s		n/a

Event recorder

Time	Type	Signal name	Slope
3,022 s	Input	DDT Etapa 0	0>1
3,033 s	Input	50BF ET0	0>1

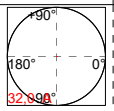
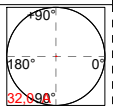
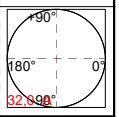
3,033 s	Output	52J3_Open	1>0
3,175 s	Input	DDT Etapa 0	1>0
3,186 s	Input	50BF ET0	1>0

Test State:

Test passed

11.2.3 Operacion End Fault_L3:

Test Settings

State	Prefalla	Falla L3+52J3 Open	Post Falla
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
52J3_Open	1	1	0
52J3_Close	0	0	0
Max. State Time	3,000 s	100,0 ms	2,000 s
Trigger Logic		AND	
DDT Etapa 0		1	
50BF ET0		1	
User interaction	no	no	no
CMGPS trigger	no	no	no
IRIG-B/PTP trigger	no	no	no
Pulses / seconds	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no
Diagrams			

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:57:38	Test End:	11-abr.-2019 01:57:44
User Name:		Manager:	
Company:			

Test Results

Time Assessment

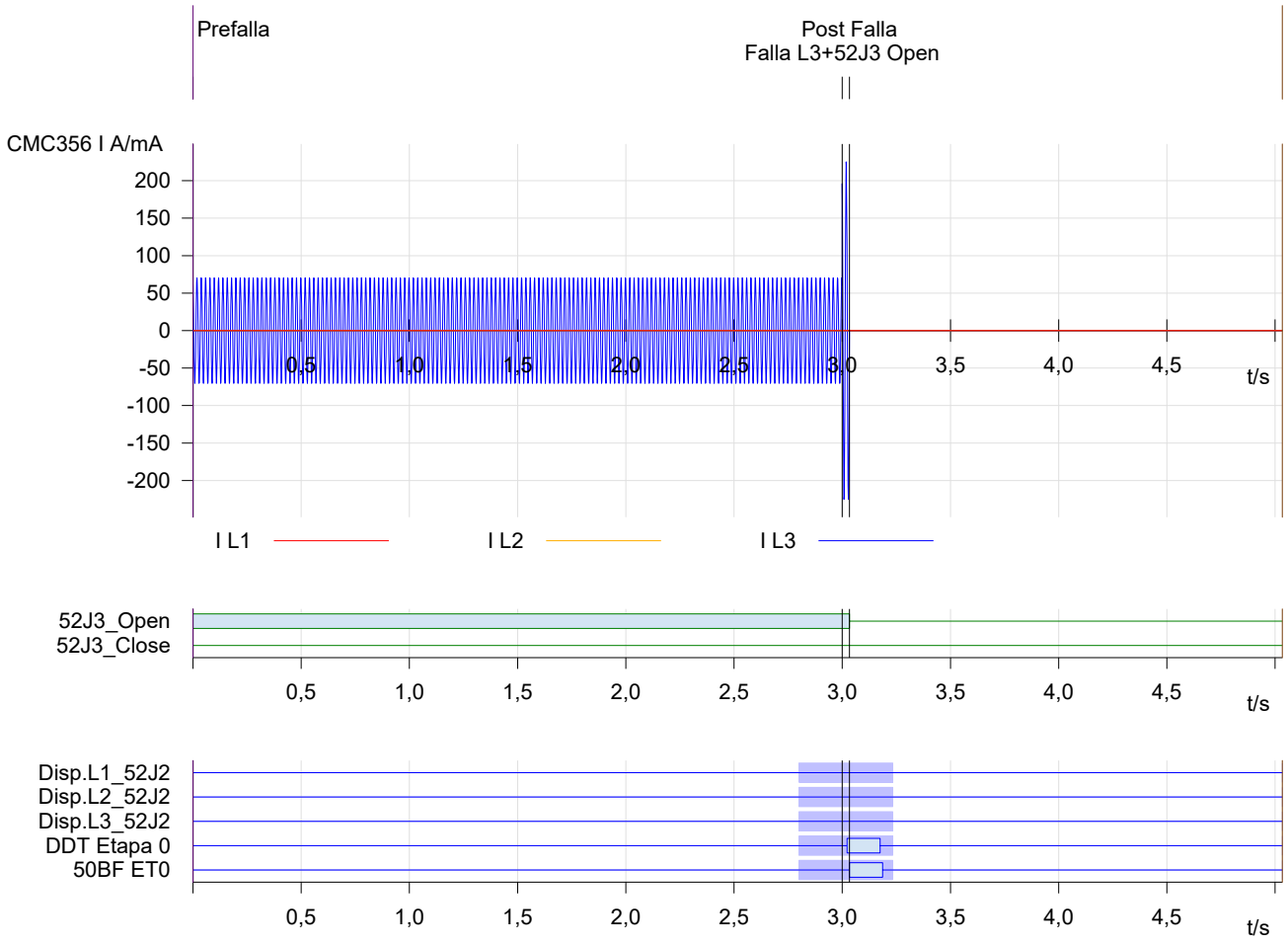
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L3+52J3 Open	Falla L3+52J3 Open	50BF ET0 0>1	50,00 ms	30,00 ms	30,00 ms	33,30 ms	-16,70 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L3+52J3 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms
Disp.L1_52J2	0	0	0
Disp.L2_52J2	0	0	0
Disp.L3_52J2	0	0	0
DDT Etapa 0	0	1	0
50BF ET0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a

Cursor 2	5,033 s	<none>	n/a
C2 - C1	5,033 s		n/a

Event recorder

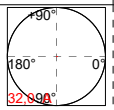
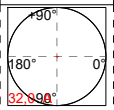
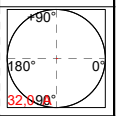
Time	Type	Signal name	Slope
3,022 s	Input	DDT Etapa 0	0>1
3,033 s	Input	50BF ET0	0>1
3,033 s	Output	52J3_Open	1>0
3,175 s	Input	DDT Etapa 0	1>0
3,187 s	Input	50BF ET0	1>0

Test State:

Test passed

12.2.4 Operacion End Fault_L123:

Test Settings

State	Prefalla	Falla L123+52J 3 Open	Post Falla
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
52J3_Open	1	1	0
52J3_Close	0	0	0
Max. State Time	3,000 s	100,0 ms	2,000 s
Trigger Logic		AND	
DDT Etapa 0		1	
50BF ET0		1	
User interaction	no	no	no
CMGPS trigger	no	no	no
IRIG-B/PTP trigger	no	no	no
Pulses / seconds	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no
Diagrams			

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:56:19	Test End:	11-abr.-2019 01:56:26
User Name:		Manager:	
Company:			

Test Results

Time Assessment

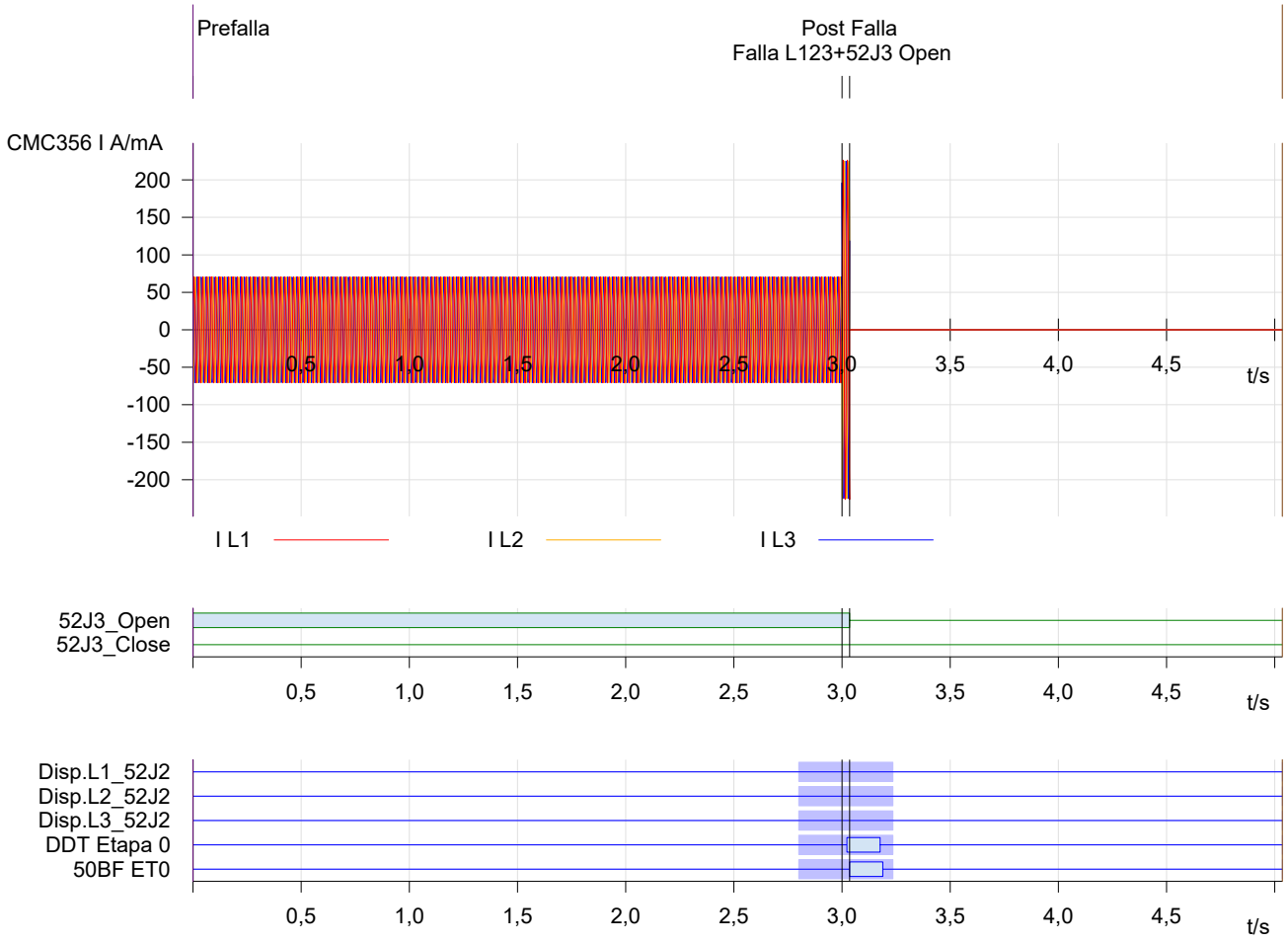
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L123+52J 3 Open	Falla L123+52J 3 Open	50BF ET0 0>1	50,00 ms	30,00 ms	30,00 ms	35,10 ms	-14,90 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L123+52J 3 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms
Disp.L1_52J2	0	0	0
Disp.L2_52J2	0	0	0
Disp.L3_52J2	0	0	0
DDT Etapa 0	0	1	0
50BF ET0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

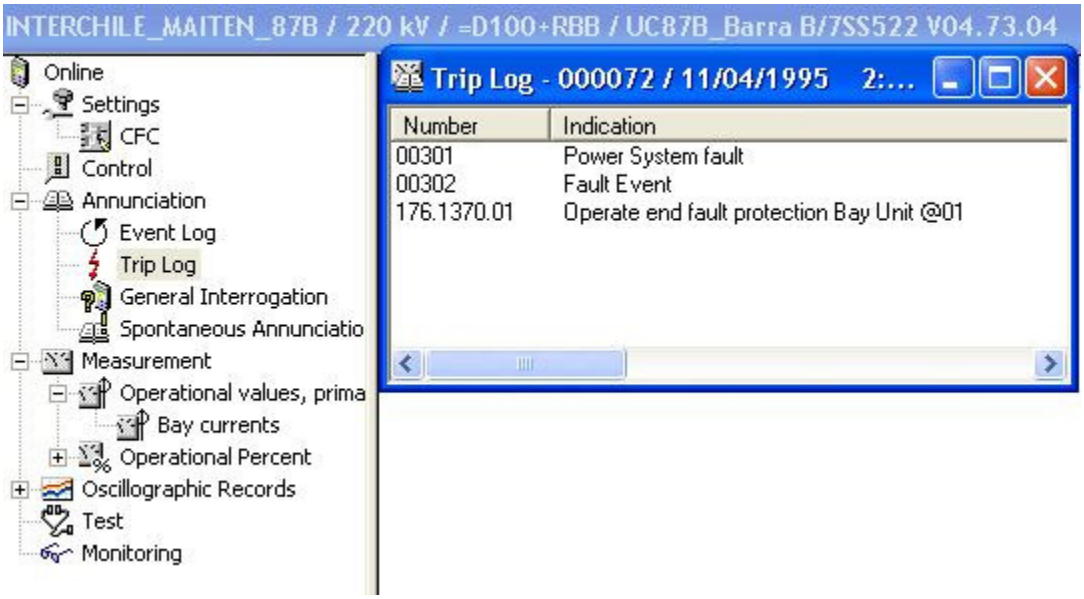
	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	5,035 s	<none>	n/a
C2 - C1	5,035 s		n/a

Event recorder

Time	Type	Signal name	Slope
3,023 s	Input	DDT Etapa 0	0>1
3,035 s	Input	50BF ET0	0>1
3,035 s	Output	52J3_Open	1>0
3,176 s	Input	DDT Etapa 0	1>0
3,188 s	Input	50BF ET0	1>0

Test State:

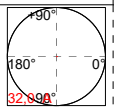
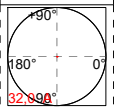
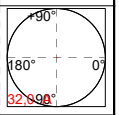
Test passed



12.2.5 Operacion End Fault_L123_CB Close:

Test Settings

State	Prefalla	Falla L123+52J 3 Open	Post Falla
I L1	50,00 mA 0,00 ° 50,000 Hz	160,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	50,00 mA -120,00 ° 50,000 Hz	160,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	50,00 mA 120,00 ° 50,000 Hz	160,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
52J3_Open	0	1	0
52J3_Close	1	0	0
Max. State Time	3,000 s	100,0 ms	2,000 s
Trigger Logic		AND	
DDT Etapa 0		1	
50BF ET0		1	

User interaction	no	no	no
CMGPS trigger	no	no	no
IRIG-B/PTP trigger	no	no	no
Pulses / seconds	1	1	1
Delay after Tr.	0,000 s	0,000 s	0,000 s
On trigger jump to test end	no	no	no
Diagrams			

Comment

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 01:59:51	Test End:	11-abr.-2019 01:59:58
User Name:		Manager:	
Company:			

Test Results

Time Assessment

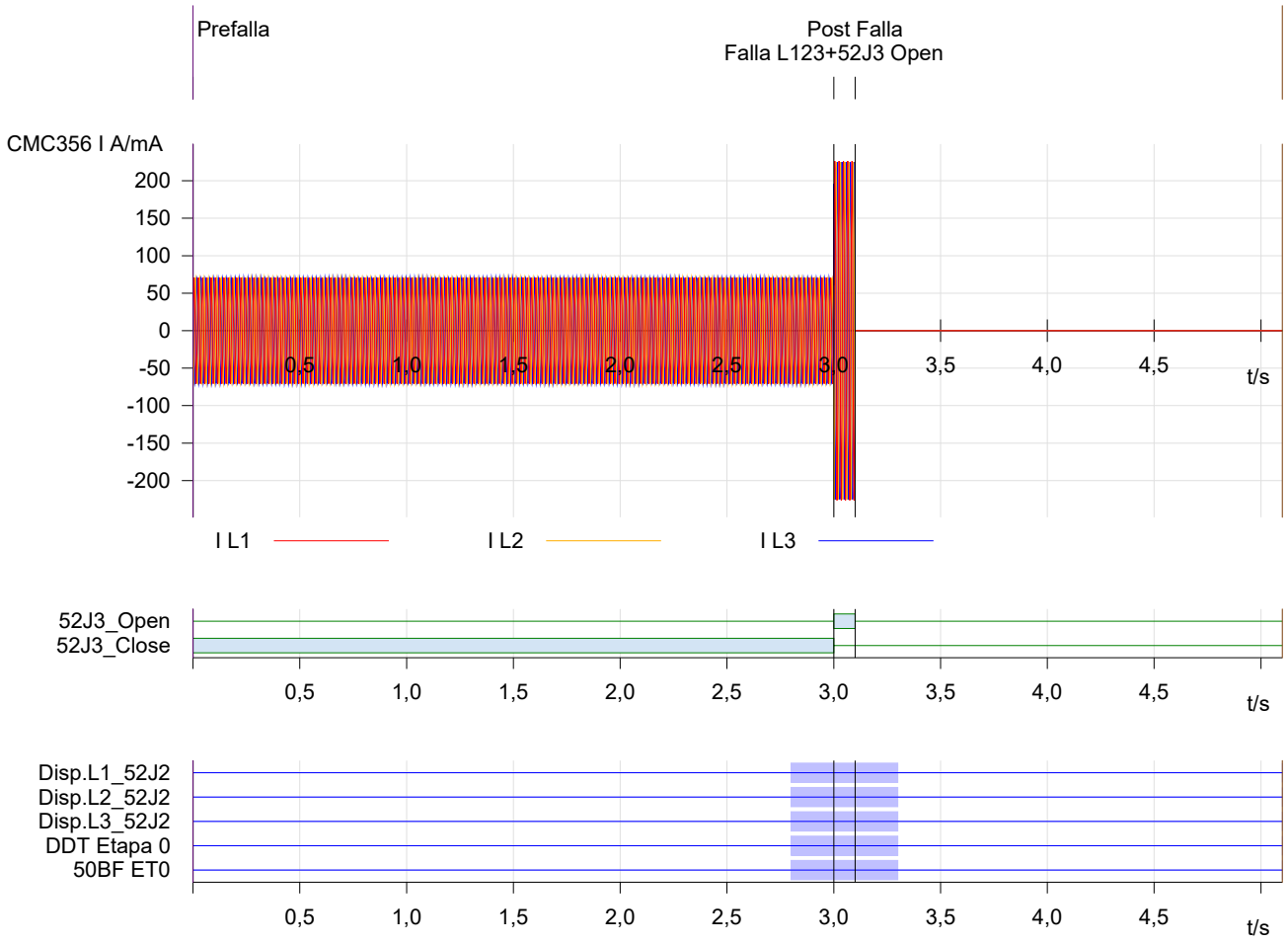
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
									o

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L123+52J 3 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms
Disp.L1_52J2	0	0	0
Disp.L2_52J2	0	0	0
Disp.L3_52J2	0	0	0
DDT Etapa 0	0	1	0
50BF ET0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	5,100 s	<none>	n/a
C2 - C1	5,100 s		n/a

Event recorder

Time	Type	Signal name	Slope
3,000 s	Output	52J3_Open	0>1
3,000 s	Output	52J3_Close	1>0
3,100 s	Output	52J3_Open	1>0

Test State:
Test passed

Group end:12.2 Operacion End Fault

Group end:12. Operacion End Fault_50BF E0

ARCHIVO DE PRUEBAS OMICRON

AUDITORIA TECNICA DE EQUIPOS DE PROTECCIONES.

PROTECCION DIFERENCIAL DE LINEA 87L, ASOCIADO AL PAÑO K11-K12 EN S/E NUEVA MAITENCILLO
MODELO 7SL87, MARCA SIEMENS

INGEMA S. A		**CLIENTE**	
Probado por: Ing. Mario Aguilar	Revisado por: Ing. Antony Porras	Recibido por:	Aprobado por:
Fecha: 12-04-2019		Fecha:	Fecha:

91SC-PP-006

Test Object - Device Settings

Substation/Bay:

Substation:	NUEVA MAITENSILLO	Substation address:	
Bay:	PAÑO K11-K12	Bay address:	

Device:

Name/description:	B04_5L24_R24_F003	Manufacturer:	SIEMENS
Device type:	7SL87	Device address:	
Serial/model number:	7SL87-DAAA-AA0-0AAAA0-AV1111-12111B-BAD000-000AA0-CH1BA1-CB1CG0-CE0		
Additional info 1:	V07.33		
Additional info 2:			

Hardware

Test Equipment

Type	Serial Number
CMC356	??????

Hardware Check

Performed At	Result	Details
Not yet performed		

Group:1. Verificacion Medida Fase L1

1.1 Inyeccion 25% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 16:58:22	Test End:	11-abr.-2019 17:00:09
User Name:		Manager:	
Company:			

Test Results

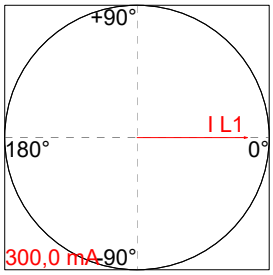
Title: Verificacion de Medida al 25% Fase A

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	250,0 mA	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,250A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



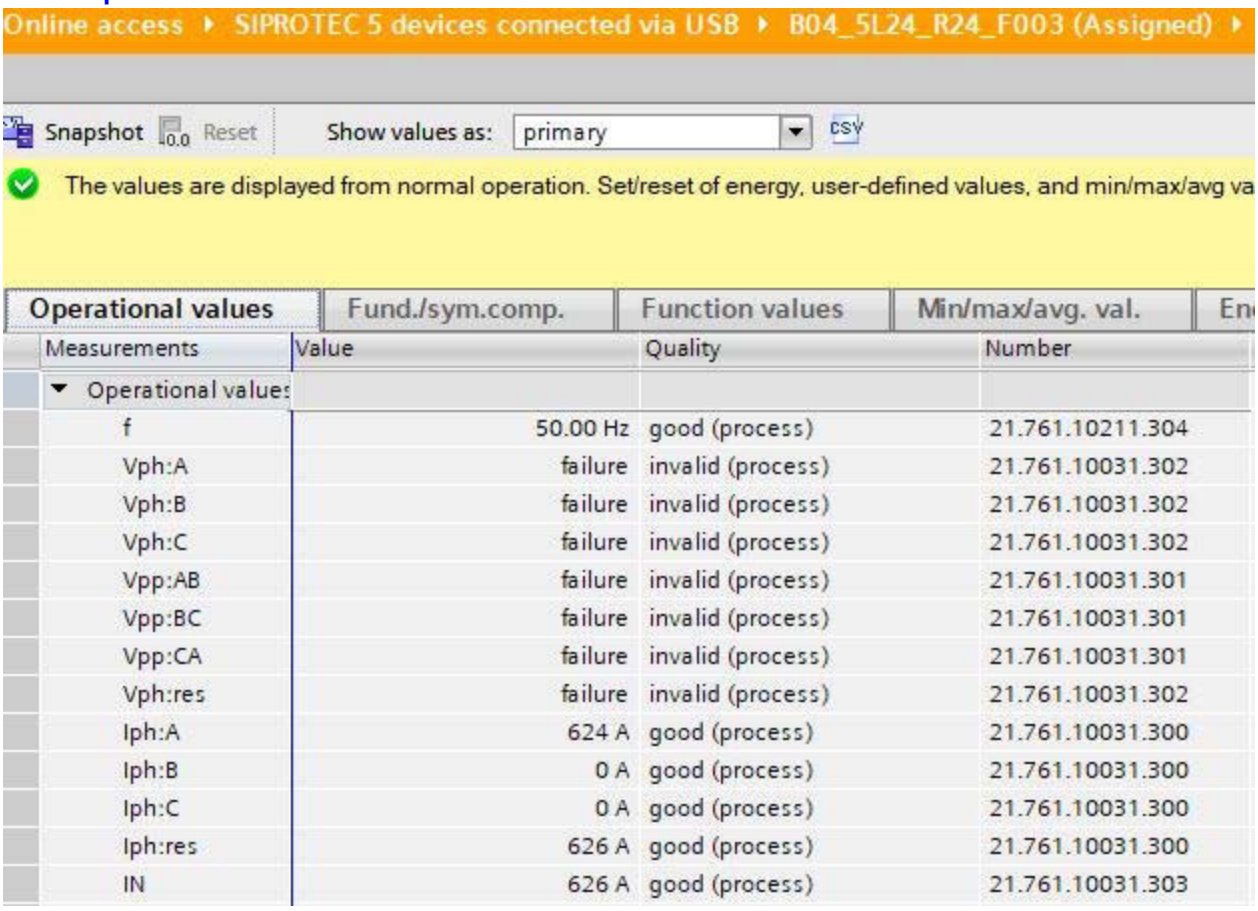
Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Measurements	Value	Quality	Number
Operational values			
f	50.00 Hz	good (process)	21.761.10211.304
Vph:A	failure	invalid (process)	21.761.10031.302
Vph:B	failure	invalid (process)	21.761.10031.302
Vph:C	failure	invalid (process)	21.761.10031.302
Vpp:AB	failure	invalid (process)	21.761.10031.301
Vpp:BC	failure	invalid (process)	21.761.10031.301
Vpp:CA	failure	invalid (process)	21.761.10031.301
Vph:res	failure	invalid (process)	21.761.10031.302
Iph:A	624 A	good (process)	21.761.10031.300
Iph:B	0 A	good (process)	21.761.10031.300
Iph:C	0 A	good (process)	21.761.10031.300
Iph:res	626 A	good (process)	21.761.10031.300
IN	626 A	good (process)	21.761.10031.303

1.2 Inyeccion 50% de Inominal:

Test Module

Name: OMICRON QuickCMC Version: 4.00

Test Start:	11-abr.-2019 17:00:15	Test End:	11-abr.-2019 17:01:00
User Name:		Manager:	
Company:			

Test Results

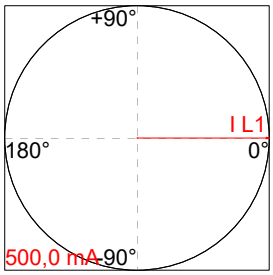
Title: Verificacion de Medida Fase A al 50%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	500,0 mA	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,500A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



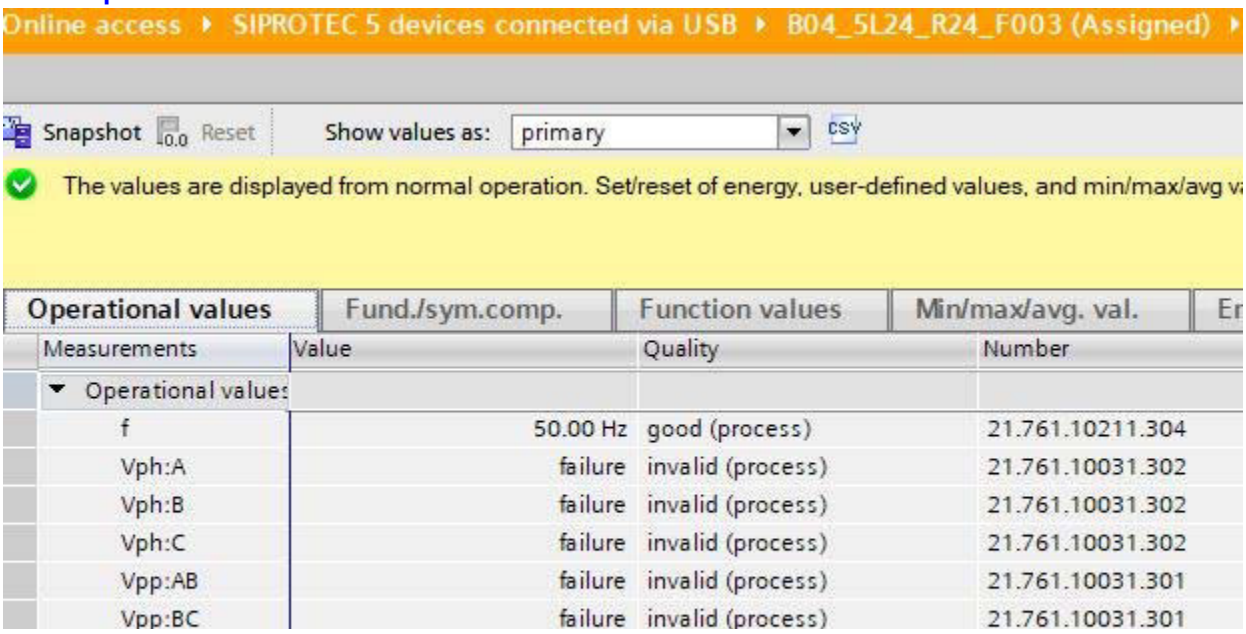
Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 17:01:05	Test End:	11-abr.-2019 17:01:39
User Name:		Manager:	
Company:			

Test Results

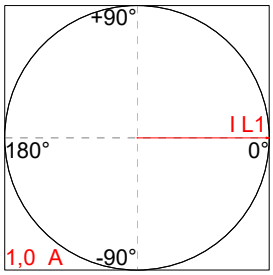
Title: Verificacion Medida Fase A al 100%

Fault Calculator:

Table Inputmode	Parameters (All values are primary)			
Direct	I L1	2,500 kA	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	2500,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



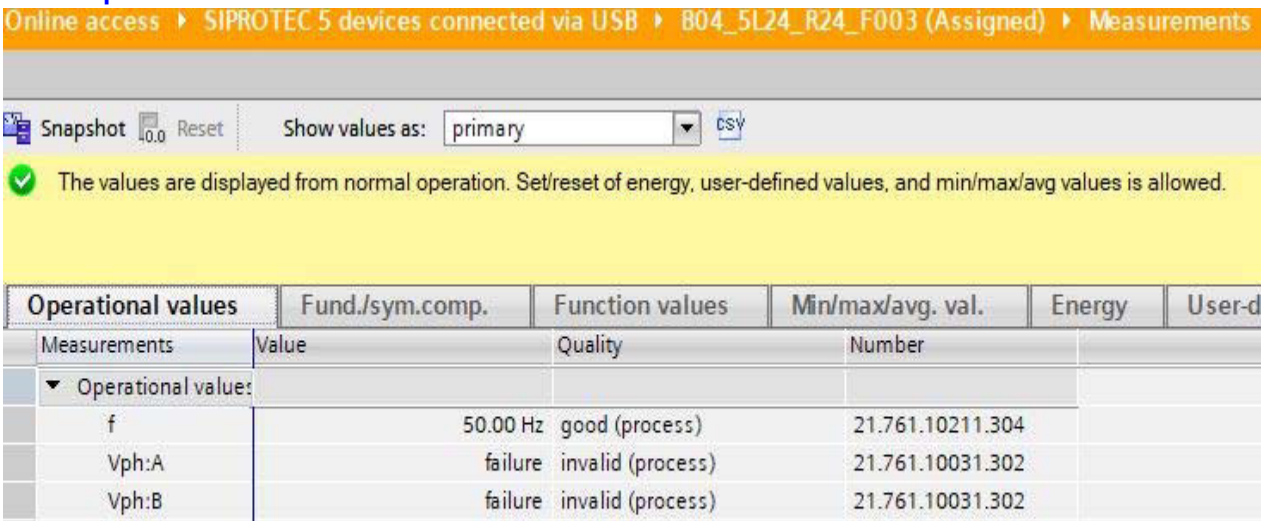
Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 17:01:47	Test End:	11-abr.-2019 17:02:23
User Name:		Manager:	
Company:			

Test Results

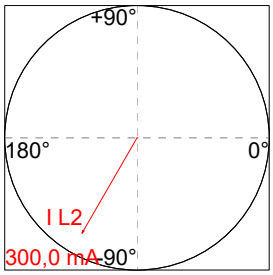
Title: Verificacion de Medida Fase B al 25%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	250,0 mA	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,250A	-120,00°
I L3	0,000A	120,00°



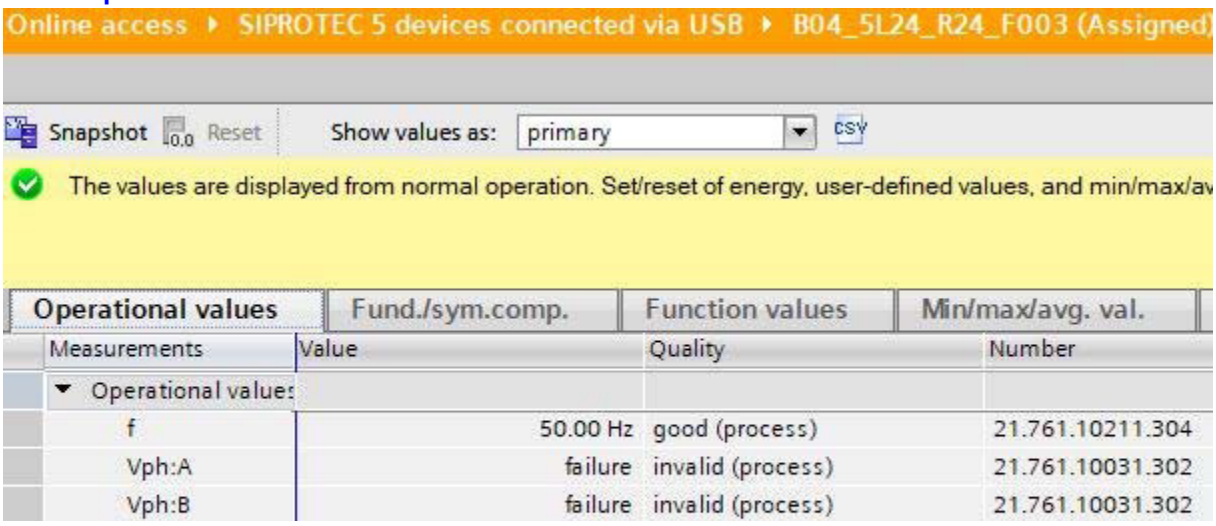
Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 17:02:30	Test End:	11-abr.-2019 17:03:29
User Name:		Manager:	
Company:			

Test Results

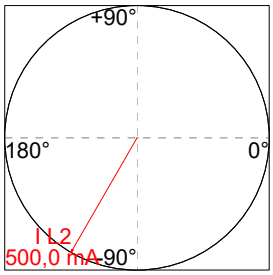
Title: Verificacion de Medida Fase B al 50%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	500,0 mA	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,500A	-120,00°
I L3	0,000A	120,00°



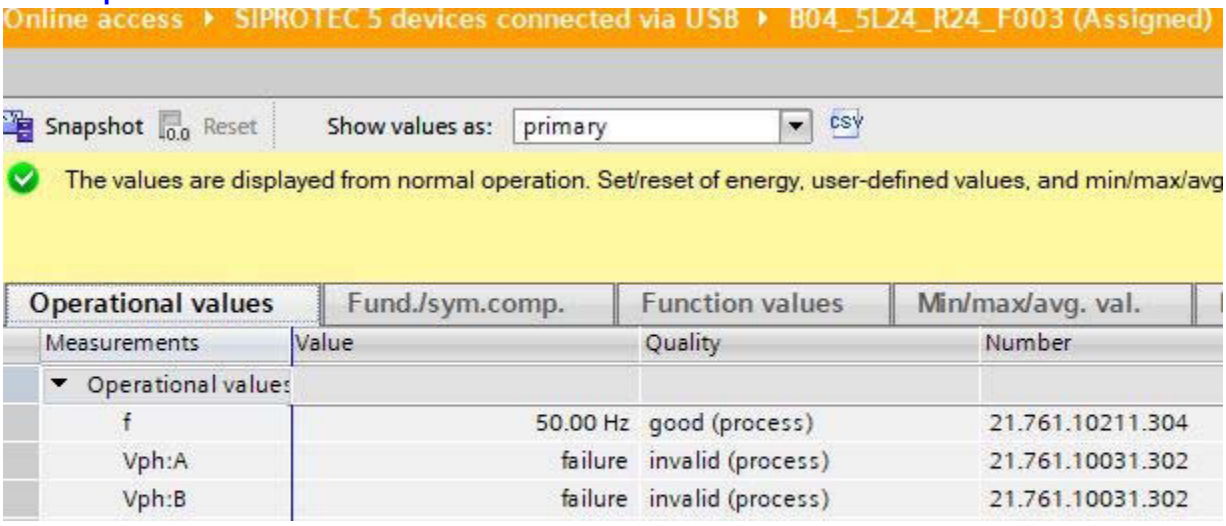
Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 17:03:34	Test End:	11-abr.-2019 17:04:08
User Name:		Manager:	
Company:			

Test Results

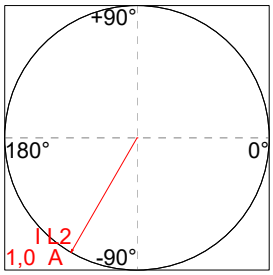
Title: Verificacion de Medida Fase B al 100%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	1,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	1,000A	-120,00°
I L3	0,000A	120,00°



Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed

Online access ▸ SIPROTEC 5 devices connected via USB ▸ B04_5L24_R24_F003 (Assigned)

Snapshot Reset Show values as: primary csv

The values are displayed from normal operation. Set/reset of energy, user-defined values, and min/max/avg

Operational values | Fund./sym.comp. | Function values | Min/max/avg. val.

Measurements	Value	Quality	Number
Operational values			
f	50.00 Hz	good (process)	21.761.10211.304
Vph:A	failure	invalid (process)	21.761.10031.302
Vph:B	failure	invalid (process)	21.761.10031.302
Vph:C	failure	invalid (process)	21.761.10031.302
Vpp:AB	failure	invalid (process)	21.761.10031.301
Vpp:BC	failure	invalid (process)	21.761.10031.301
Vpp:CA	failure	invalid (process)	21.761.10031.301

Group end:2. Verificacion Medida Fase L2

Group:3. Verificacion Medida Fase L3

3.1 Inyeccion 25% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 17:04:23	Test End:	11-abr.-2019 17:04:55
User Name:		Manager:	
Company:			

Test Results

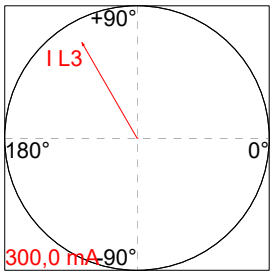
Title: Verificacion de Medida Fase C al 25%

Fault Calculator:

Table Inputmode	Parameters (All values are primary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	625,0 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	625,000A	120,00°



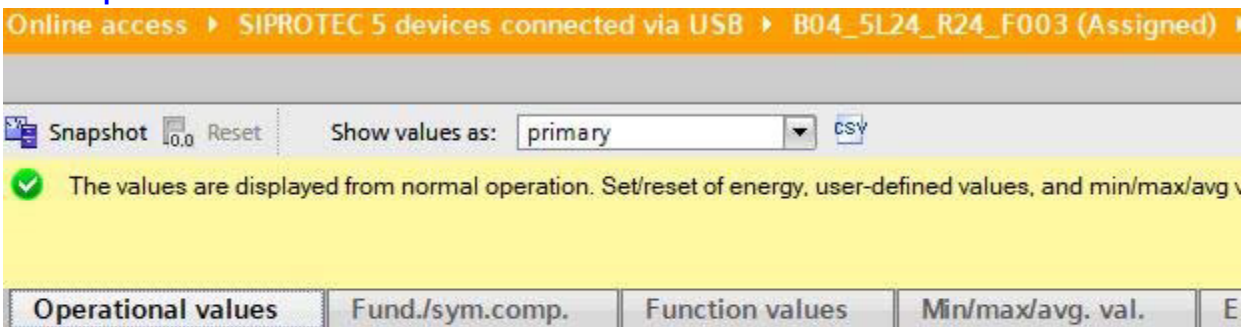
Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 17:05:00	Test End:	11-abr.-2019 17:05:35
User Name:		Manager:	
Company:			

Test Results

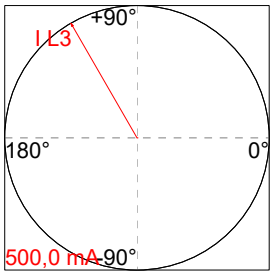
Title: Verificacion Medida Fase C al 50%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	500,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,500A	120,00°



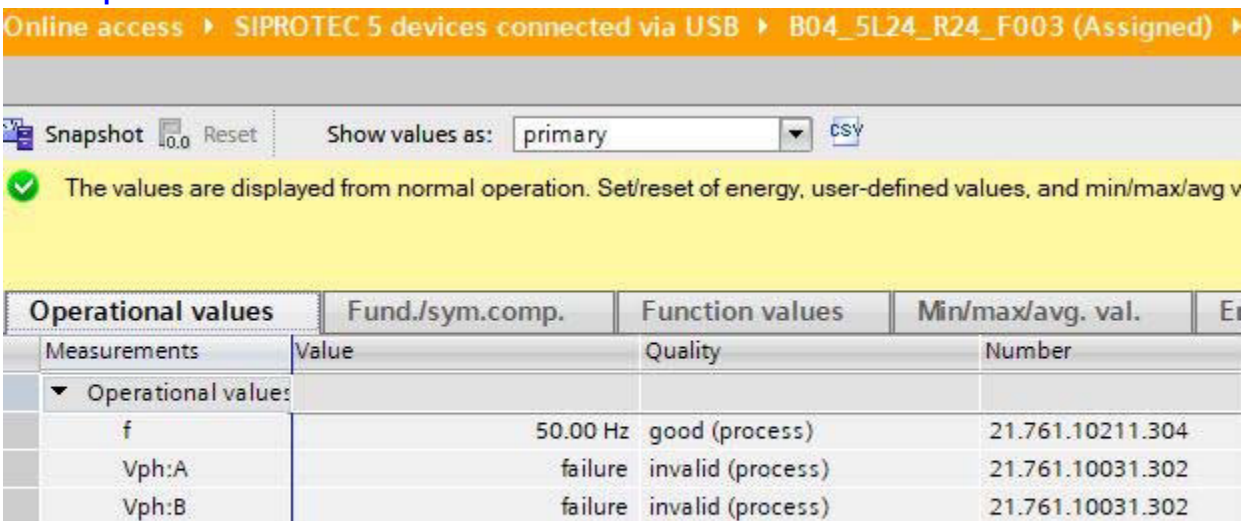
Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 17:05:42	Test End:	11-abr.-2019 17:06:12
User Name:		Manager:	
Company:			

Test Results

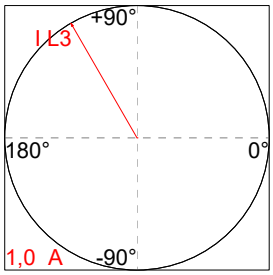
Title: Verificacion Msedida Fase C al 100%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	1,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	1,000A	120,00°



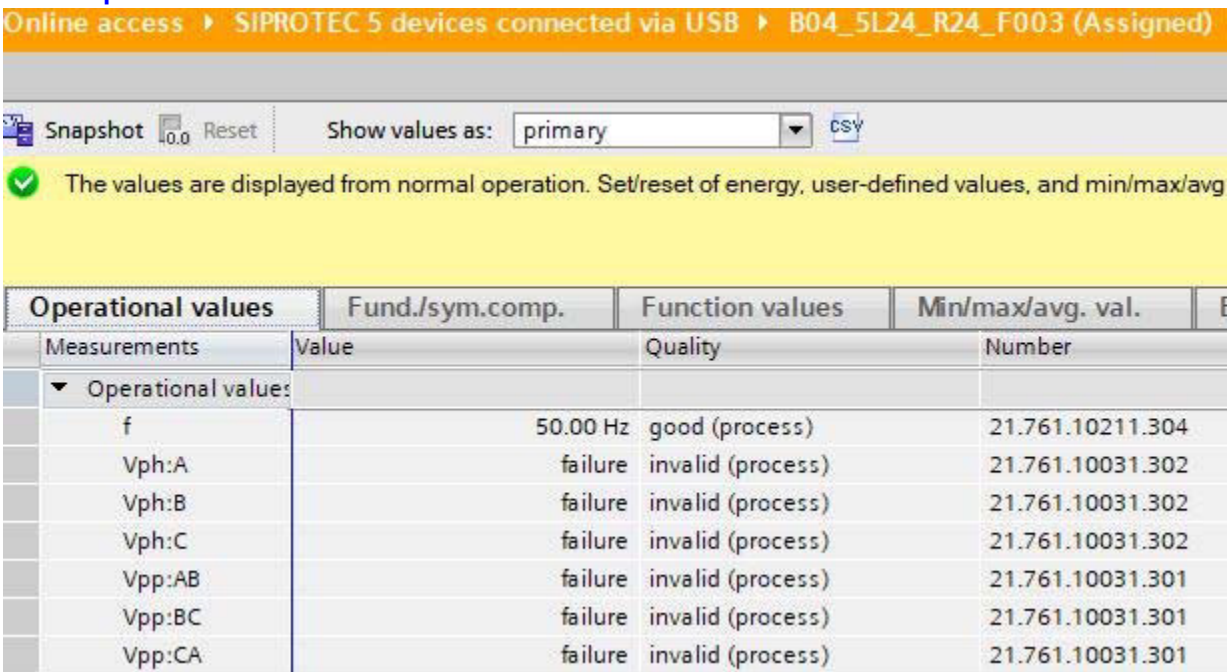
Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:3. Verificacion Medida Fase L3

Group:4. Verificacion Medida Fases L123

4.1 Inyeccion 25% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 17:06:19	Test End:	11-abr.-2019 17:06:58
User Name:		Manager:	
Company:			

Test Results

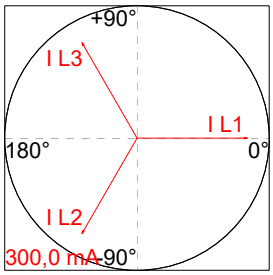
Title: Verificacion Medida Fases ABC al 25%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	250,0 mA	0,00 °	50,000 Hz
	I L2	250,0 mA	-120,00 °	50,000 Hz
	I L3	250,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,250A	0,00°
I L2	0,250A	-120,00°
I L3	0,250A	120,00°



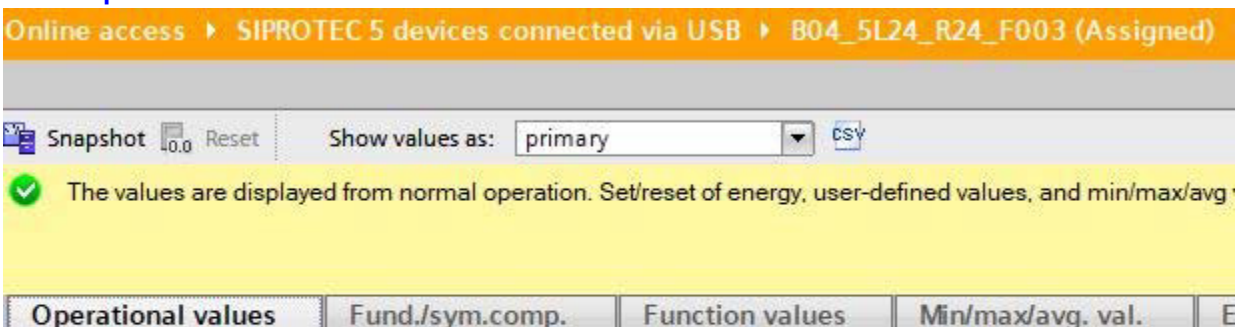
Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 17:07:03	Test End:	11-abr.-2019 17:07:44
User Name:		Manager:	
Company:			

Test Results

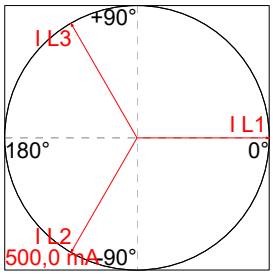
Title: Verificacion Medida Fases ABC al 50%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	500,0 mA	0,00 °	50,000 Hz
	I L2	500,0 mA	-120,00 °	50,000 Hz
	I L3	500,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,500A	0,00°
I L2	0,500A	-120,00°
I L3	0,500A	120,00°



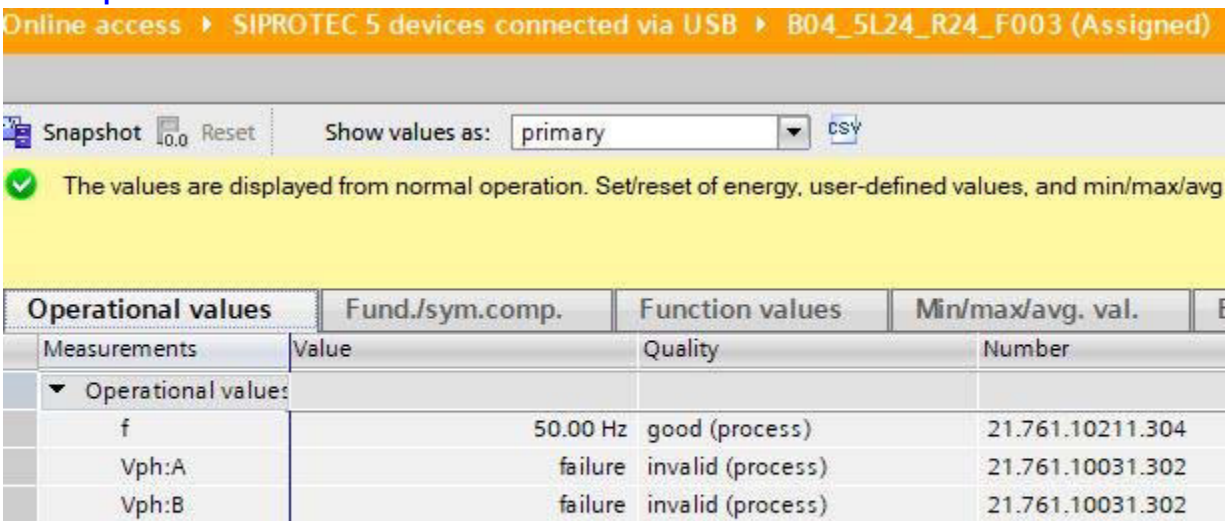
Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	11-abr.-2019 17:07:52	Test End:	11-abr.-2019 17:08:33
User Name:		Manager:	
Company:			

Test Results

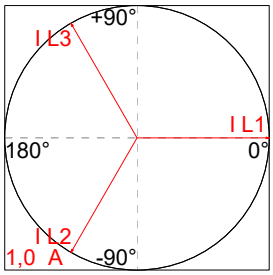
Title: Verifiacion Medida Fases ABC al 100%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	1,000 A	0,00 °	50,000 Hz
	I L2	1,000 A	-120,00 °	50,000 Hz
	I L3	1,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	1,000A	0,00°
I L2	1,000A	-120,00°
I L3	1,000A	120,00°



Binary Inputs

Name	Slope	Time
TRIP-L1_K11	1	
TRIP-L2_K11	1	
TRIP-L3_K11	1	
TRIP-L1_K12	0	
TRIP-L2_K12	0	
TRIP-L3_K12	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed

Online access ▸ SIPROTEC 5 devices connected via USB ▸ B04_5L24_R24_F003 (Assigned)

Snapshot Reset Show values as: primary csv

The values are displayed from normal operation. Set/reset of energy, user-defined values, and min/max/avg

Operational values | Fund./sym.comp. | Function values | Min/max/avg. val.

Measurements	Value	Quality	Number
Operational values			
f	50.00 Hz	good (process)	21.761.10211.304
Vph:A	failure	invalid (process)	21.761.10031.302
Vph:B	failure	invalid (process)	21.761.10031.302
Vph:C	failure	invalid (process)	21.761.10031.302
Vpp:AB	failure	invalid (process)	21.761.10031.301
Vpp:BC	failure	invalid (process)	21.761.10031.301
Vpp:CA	failure	invalid (process)	21.761.10031.301

Group end:4. Verificacion Medida Fases L123

Group:5.- Arranque 87L

5.1 Arranque L1:

Test Settings

General

No. of ramp states:	1
Total steps per test:	10
Total time per test:	5,000 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	0,000 A
Sig 1 To	500,0 mA
Sig 1 Delta	60,00 mA
Sig 1 d/dt	120,0 mA/s
dt per Step	500,0 ms
Ramp Steps	10
Ramp Time	5,000s
Trigger	Bin
Trigger Logic	AND
TRIP-L1_K11	1
TRIP-L2_K11	1
TRIP-L3_K11	1
TRIP-L1_K12	1
TRIP-L2_K12	1
TRIP-L3_K12	1
Step back	No
Delay Time	1,000 s

Test Module

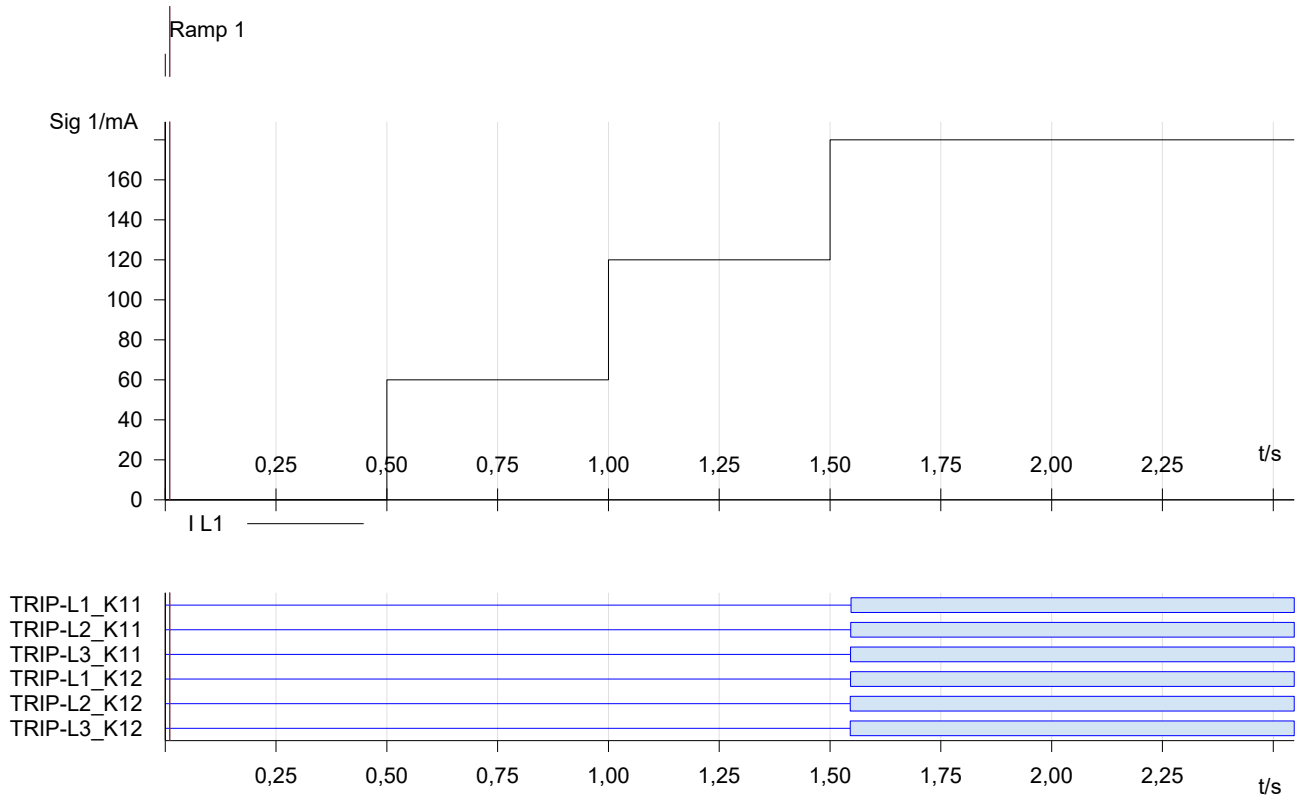
Name:	OMICRON Ramping	Version:	4.00

Test Start:	11-abr.-2019 19:32:55	Test End:	11-abr.-2019 19:32:59
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Arranque L1	Ramp 1	TRIP-L2_K11 0->1 and TRIP-L3_K11 0->1 and TRIP-L1_K12 0->1 and TRIP-L2_K12 0->1 and TRIP-L3_K12 0->1 and TRIP-L1_K11 0->1	I L1	170,0 mA	180,0 mA	20,00 mA	20,00 mA	10,00 mA	+	47,30 ms

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	10,00 ms	I L1	0,00 A
Cursor 2	10,00 ms	I L1	0,00 A
C2 - C1	0,000 s	I L1 - I L1	0,00 A

Test State:
Test passed

5.2 Arranque L2:

Test Settings

General

No. of ramp states:	1
Total steps per test:	10
Total time per test:	5,000 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	0,000 A
Sig 1 To	500,0 mA
Sig 1 Delta	60,00 mA
Sig 1 d/dt	120,0 mA/s
dt per Step	500,0 ms
Ramp Steps	10
Ramp Time	5,000s
Trigger	Bin
Trigger Logic	AND
TRIP-L1_K11	1
TRIP-L2_K11	1
TRIP-L3_K11	1
TRIP-L1_K12	1
TRIP-L2_K12	1
TRIP-L3_K12	1
Step back	No
Delay Time	1,000 s

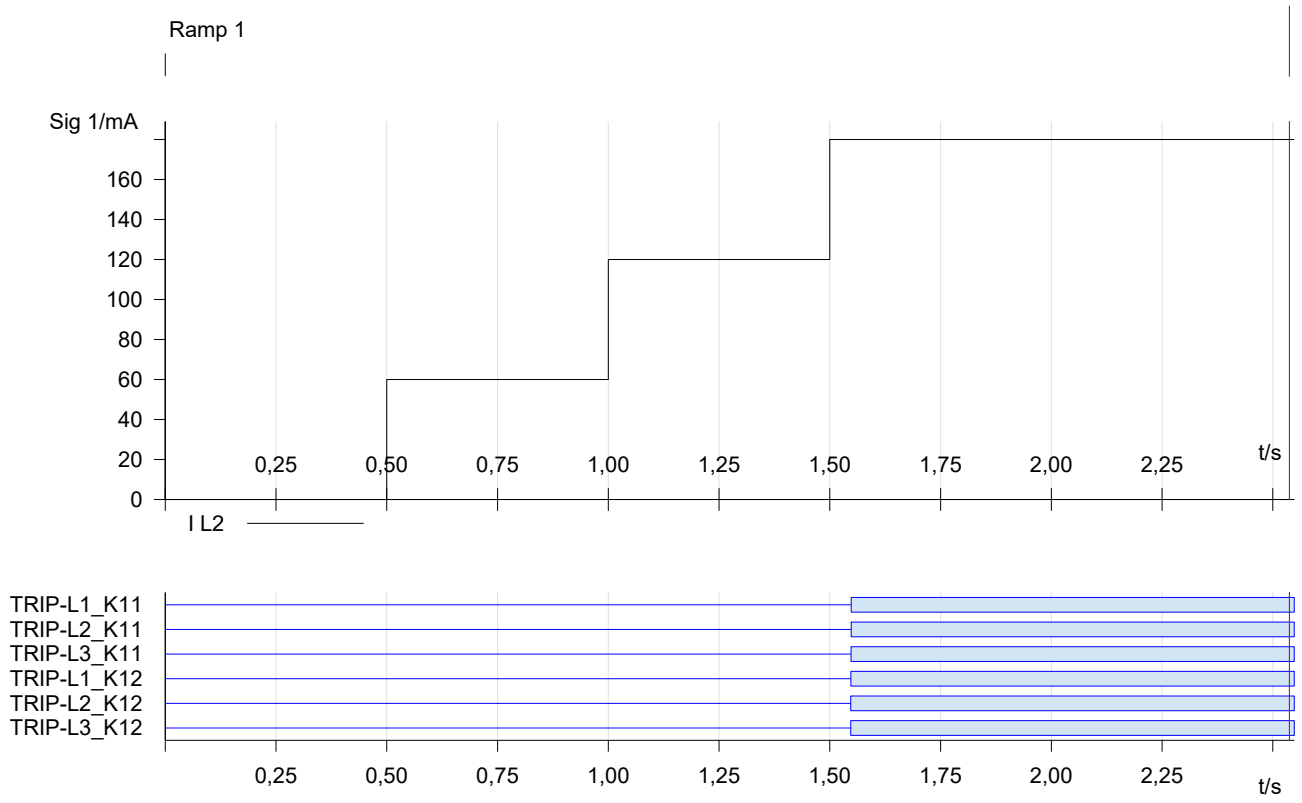
Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 19:37:11	Test End:	11-abr.-2019 19:37:16
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Arranque L2	Ramp 1	TRIP-L1_K11 0->1 and TRIP-L2_K11 0->1 and TRIP-L3_K11 0->1 and TRIP-L1_K12 0->1 and TRIP-L2_K12 0->1 and TRIP-L3_K12 0->1	I L2	170,0 mA	180,0 mA	20,00 mA	20,00 mA	10,00 mA	+	48,20 ms

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	2,538 s	<none>	n/a
Cursor 2	2,538 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:

Test passed

5.3 Arranque L3:

Test Settings

General

No. of ramp states: 1
Total steps per test: 10
Total time per test: 5,000 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	0,000 A
Sig 1 To	500,0 mA
Sig 1 Delta	60,00 mA
Sig 1 d/dt	120,0 mA/s
dt per Step	500,0 ms
Ramp Steps	10
Ramp Time	5,000s
Trigger	Bin
Trigger Logic	AND
TRIP-L1_K11	1
TRIP-L2_K11	1
TRIP-L3_K11	1
TRIP-L1_K12	1
TRIP-L2_K12	1
TRIP-L3_K12	1
Step back	No
Delay Time	1,000 s

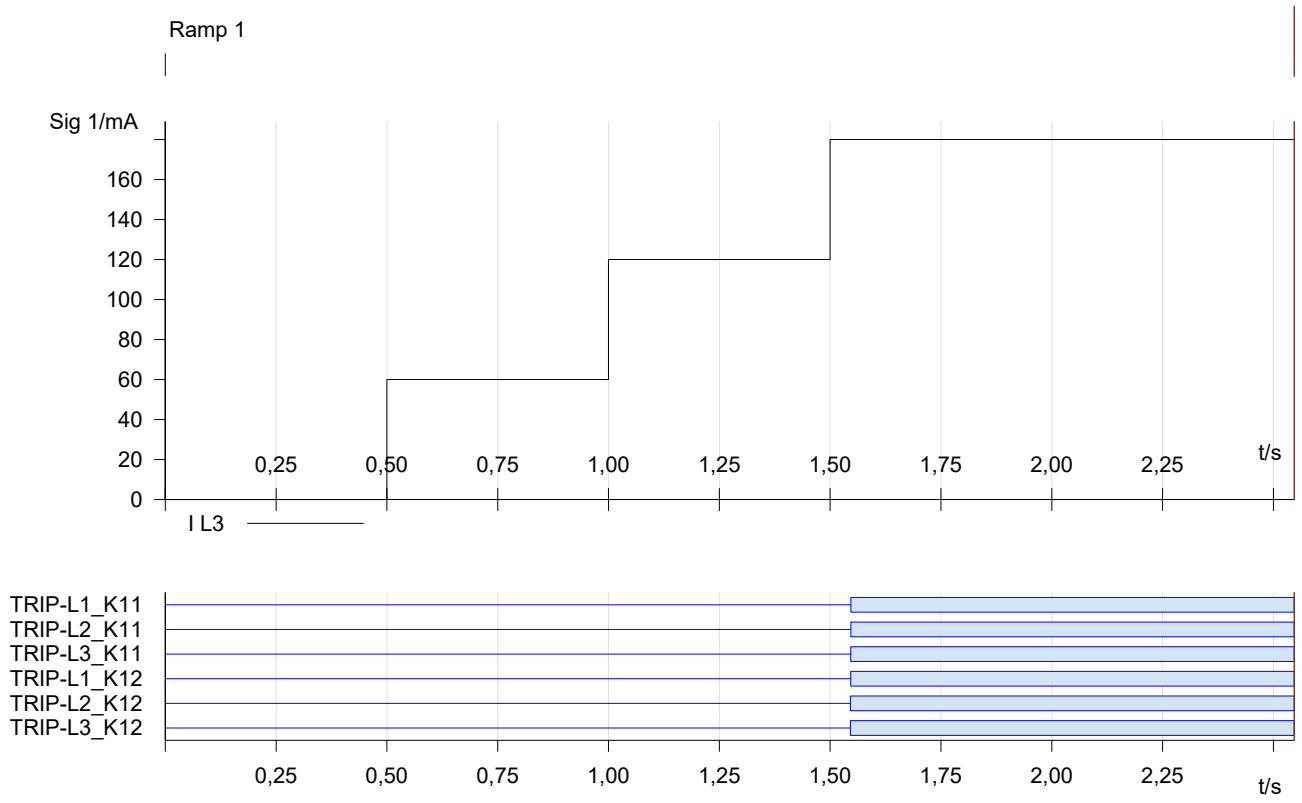
Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 19:25:24
Test End: 11-abr.-2019 19:25:29
User Name:
Manager:
Company:

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Arranque L3	Ramp 1	TRIP-L1_K11 0->1 and TRIP-L2_K11 0->1 and TRIP-L3_K11 0->1 and TRIP-L1_K12 0->1 and TRIP-L2_K12 0->1 and TRIP-L3_K12 0->1	I L3	170,0 mA	180,0 mA	20,00 mA	20,00 mA	10,00 mA	+	46,90 ms

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	2,547 s	<none>	n/a
Cursor 2	2,547 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:

Test passed

5.4 Arranque L1-L2:

Test Settings

General

No. of ramp states:	1
Total steps per test:	10
Total time per test:	5,000 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L1; L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	0,000 A
Sig 1 To	500,0 mA
Sig 1 Delta	60,00 mA
Sig 1 d/dt	120,0 mA/s
dt per Step	500,0 ms
Ramp Steps	10
Ramp Time	5,000s
Trigger	Bin
Trigger Logic	AND
TRIP-L1_K11	1
TRIP-L2_K11	1
TRIP-L3_K11	1
TRIP-L1_K12	1
TRIP-L2_K12	1
TRIP-L3_K12	1
Step back	No
Delay Time	1,000 s

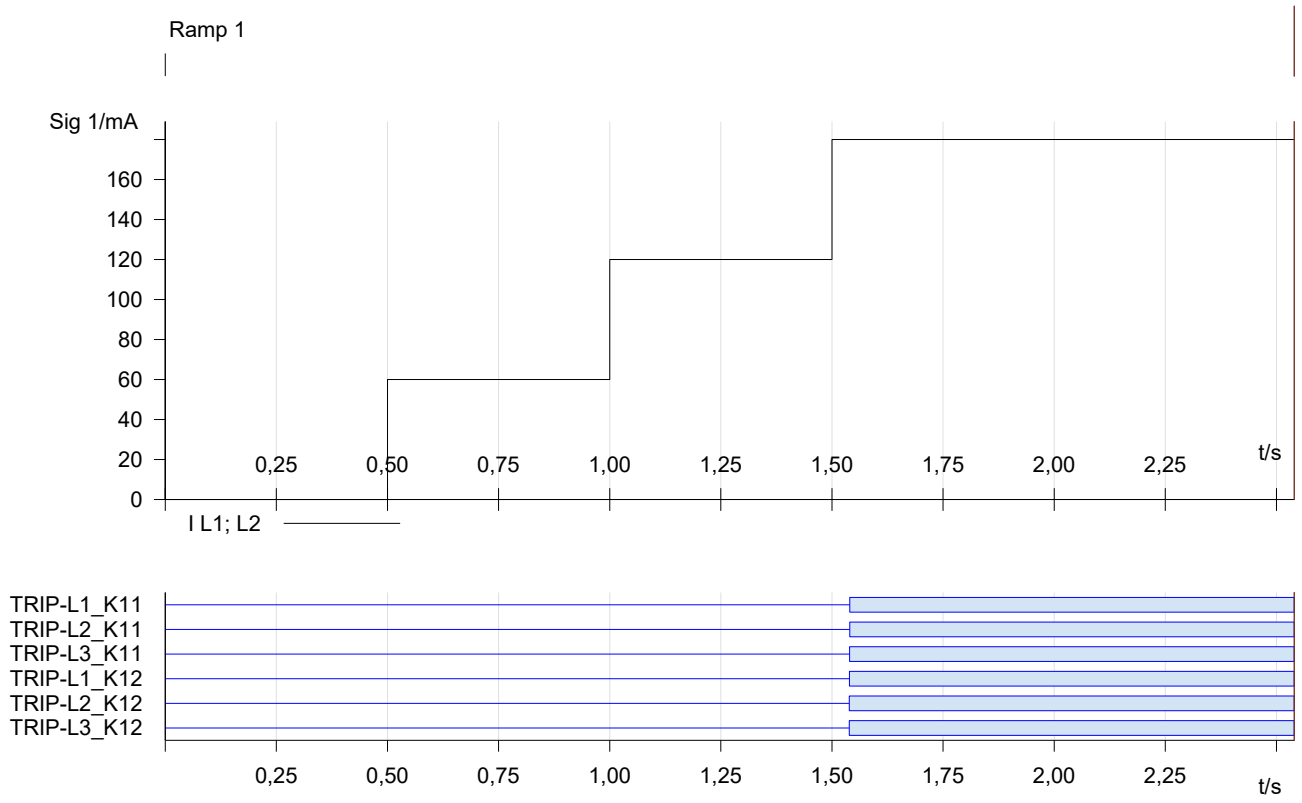
Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 19:37:50	Test End:	11-abr.-2019 19:37:54
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Arranque L1-L2	Ramp 1	TRIP-L1_K11 0->1 and TRIP-L2_K11 0->1 and TRIP-L3_K11 0->1 and TRIP-L1_K12 0->1 and TRIP-L2_K12 0->1 and TRIP-L3_K12 0->1	I L1; L2	170,0 mA	180,0 mA	20,00 mA	20,00 mA	10,00 mA	+	40,00 ms

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	2,540 s	<none>	n/a
Cursor 2	2,540 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:

Test passed

5.5 Arranque L2-L3:

Test Settings

General

No. of ramp states:	1
Total steps per test:	10
Total time per test:	5,000 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	0,000 A
Sig 1 To	500,0 mA
Sig 1 Delta	60,00 mA
Sig 1 d/dt	120,0 mA/s
dt per Step	500,0 ms
Ramp Steps	10
Ramp Time	5,000s
Trigger	Bin
Trigger Logic	AND
TRIP-L1_K11	1
TRIP-L2_K11	1
TRIP-L3_K11	1
TRIP-L1_K12	1
TRIP-L2_K12	1
TRIP-L3_K12	1
Step back	No
Delay Time	1,000 s

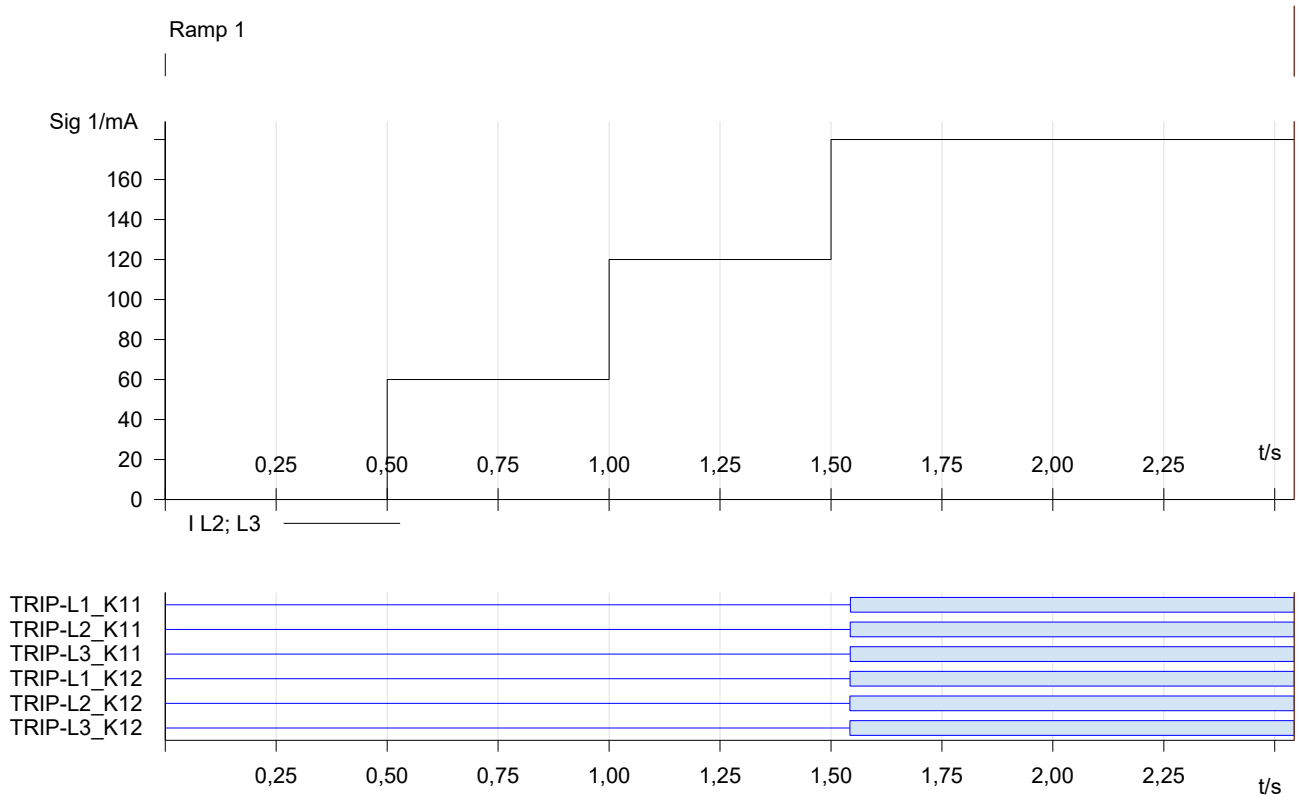
Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 19:38:12	Test End:	11-abr.-2019 19:38:17
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Arranque L1-L2	Ramp 1	TRIP-L1_K11 0->1 and TRIP-L2_K11 0->1 and TRIP-L3_K11 0->1 and TRIP-L1_K12 0->1 and TRIP-L2_K12 0->1 and TRIP-L3_K12 0->1	I L2; L3	170,0 mA	180,0 mA	20,00 mA	20,00 mA	10,00 mA	+	43,80 ms

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	2,544 s	<none>	n/a
Cursor 2	2,544 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:

Test passed

5.6 Arranque L3-L1:

Test Settings

General

No. of ramp states:	1
Total steps per test:	10
Total time per test:	5,000 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L3; L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	0,000 A
Sig 1 To	500,0 mA
Sig 1 Delta	60,00 mA
Sig 1 d/dt	120,0 mA/s
dt per Step	500,0 ms
Ramp Steps	10
Ramp Time	5,000s
Trigger	Bin
Trigger Logic	AND
TRIP-L1_K11	1
TRIP-L2_K11	1
TRIP-L3_K11	1
TRIP-L1_K12	1
TRIP-L2_K12	1
TRIP-L3_K12	1
Step back	No
Delay Time	1,000 s

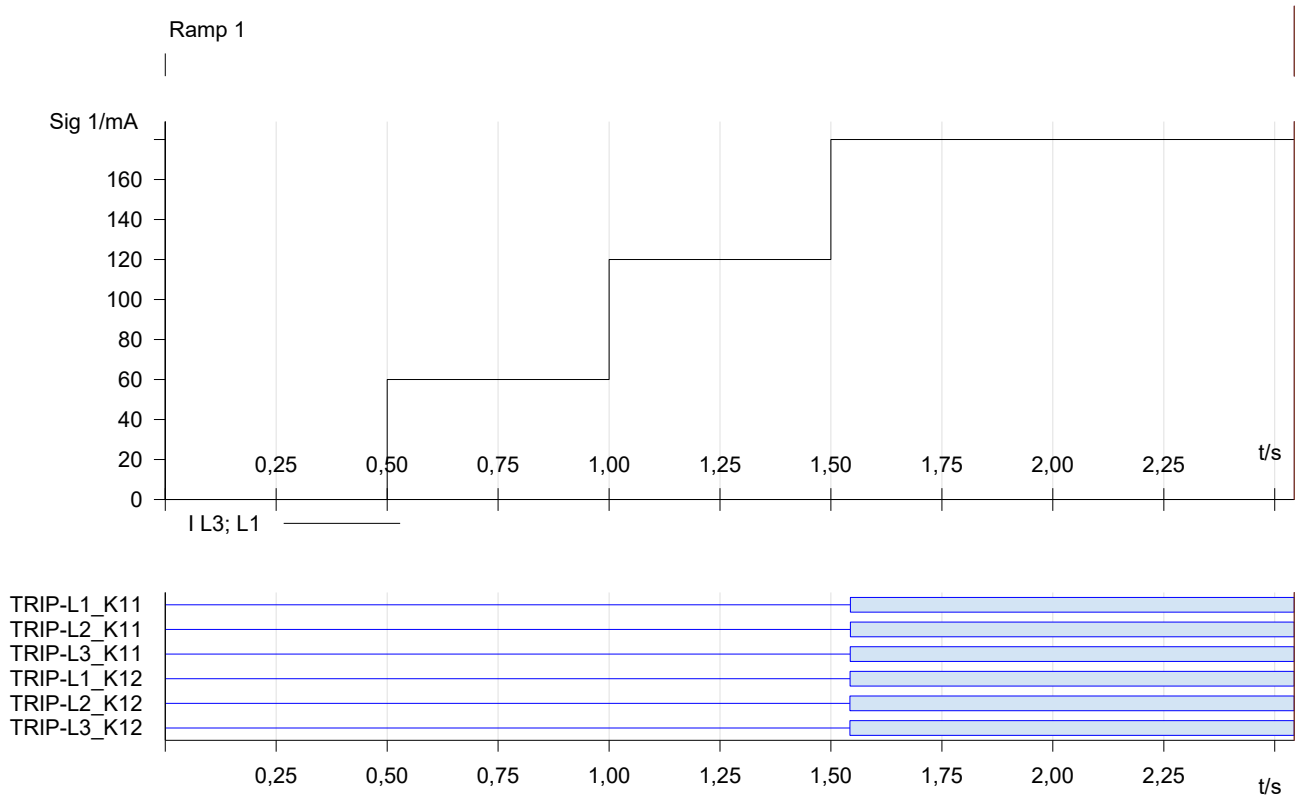
Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	11-abr.-2019 19:06:46	Test End:	11-abr.-2019 19:06:50
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Arranque L1-L2	Ramp 1	TRIP-L1_K11 0->1 and TRIP-L2_K11 0->1 and TRIP-L3_K11 0->1 and TRIP-L1_K12 0->1 and TRIP-L2_K12 0->1 and TRIP-L3_K12 0->1	I L3; L1	170,0 mA	180,0 mA	20,00 mA	20,00 mA	10,00 mA	+	43,90 ms

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	2,544 s	<none>	n/a
Cursor 2	2,544 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:

Test passed

5.7 Arranque L1-L2-L3:

Test Settings

General

No. of ramp states: 1
Total steps per test: 10
Total time per test: 5,000 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	Yes
Sig 1 From	0,000 A
Sig 1 To	500,0 mA
Sig 1 Delta	60,00 mA
Sig 1 d/dt	120,0 mA/s
dt per Step	500,0 ms
Ramp Steps	10
Ramp Time	5,000s
Trigger	Bin
Trigger Logic	AND
TRIP-L1_K11	1
TRIP-L2_K11	1
TRIP-L3_K11	1
TRIP-L1_K12	1
TRIP-L2_K12	1
TRIP-L3_K12	1
Step back	No
Delay Time	1,000 s

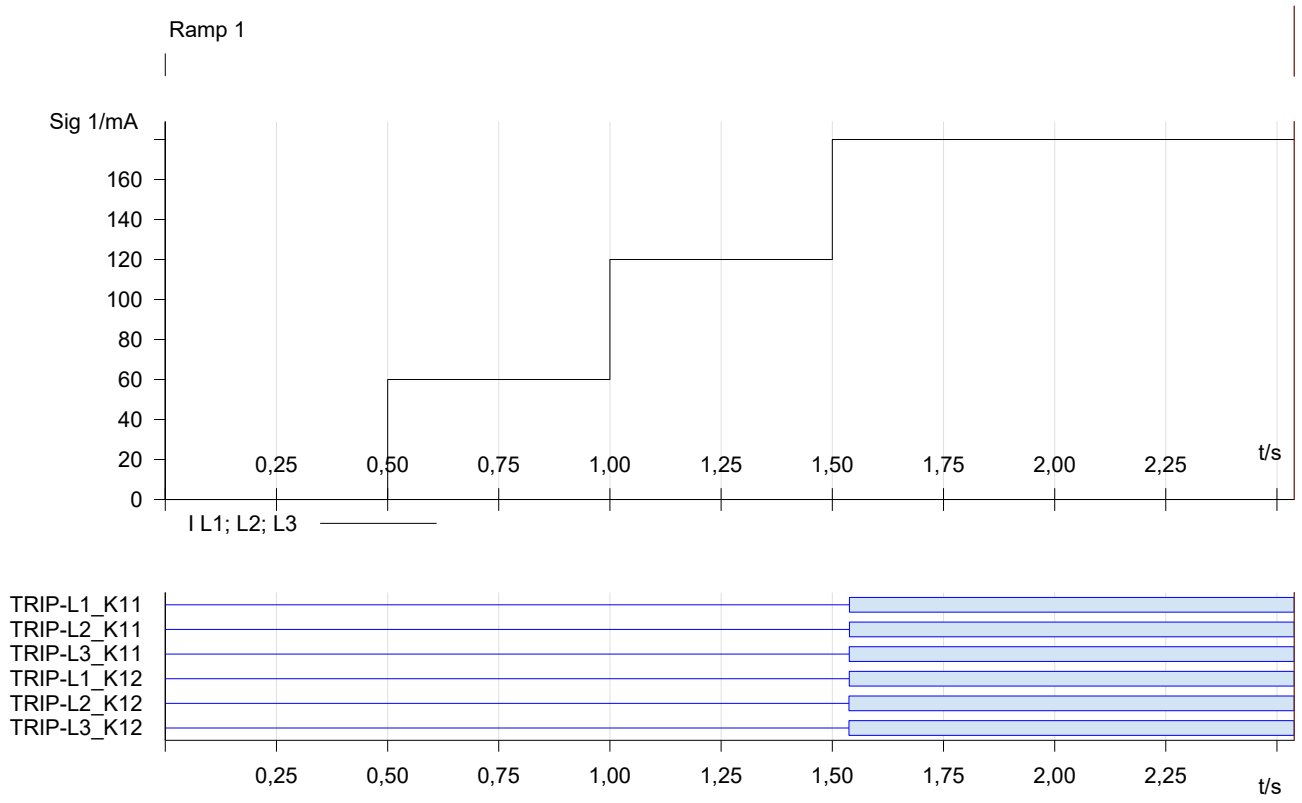
Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 11-abr.-2019 19:07:26
Test End: 11-abr.-2019 19:07:30
User Name:
Manager:
Company:

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Arranque L1-L2	Ramp 1	TRIP-L1_K11 0->1 and TRIP-L2_K11 0->1 and TRIP-L3_K11 0->1 and TRIP-L1_K12 0->1 and TRIP-L2_K12 0->1 and TRIP-L3_K12 0->1	I L1; L2; L3	170,0 mA	180,0 mA	20,00 mA	20,00 mA	10,00 mA	+	38,70 ms

Assess: + .. Passed x .. Failed o .. Not assessed



Cursor Data

	Time	Signal	Value
Cursor 1	2,539 s	<none>	n/a
Cursor 2	2,539 s	<none>	n/a
C2 - C1	0,000 s		n/a

Test State:

Test passed

5.8 Tiempo Actuación 87L_ Falla L1:

Test Settings

State	Pre-Falla	Falla Fase L1	Post-Falla
I L1	100,0 mA 0,00 ° 50,000 Hz	1,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	100,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	100,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 19:12:18	Test End:	11-abr.-2019 19:12:23
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Tiempo_87L	Falla Fase L1	Falla Fase L1	TRIP-L1_K11 0>1	30,00 ms	20,00 ms	20,00 ms	42,30 ms	12,30 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Pre-Falla	Falla Fase L1	Post-Falla
Assess	+	+	+
Tolerance	0,000 s	100,0 ms	200,0 ms
TRIP-L1_K11	0	1	0
TRIP-L2_K11	0	1	0
TRIP-L3_K11	0	1	0
TRIP-L1_K12	0	1	0
TRIP-L2_K12	0	1	0
TRIP-L3_K12	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

5.9 Tiempo Actuación 87L_ Falla L2:

Test Settings

State	Pre-Falla	Falla Fase L2	Post-Falla
I L1	100,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz

I L2	100,0 mA -120,00 ° 50,000 Hz	1,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	100,0 mA 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 19:29:22	Test End:	11-abr.-2019 19:29:27
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Tiempo_87L	Falla Fase L2	Falla Fase L2	TRIP-L2_K12 0>1	30,00 ms	20,00 ms	20,00 ms	36,80 ms	6,800 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Pre-Falla	Falla Fase L2	Post-Falla
Assess	+	+	+
Tolerance	0,000 s	100,0 ms	200,0 ms
TRIP-L1_K11	0	1	0
TRIP-L2_K11	0	1	0
TRIP-L3_K11	0	1	0
TRIP-L1_K12	0	1	0
TRIP-L2_K12	0	1	0
TRIP-L3_K12	0	1	0
Start_50BF K11	0	1	0
Release 50BF_K11	0	1	0
Start_50BF K12	0	1	0
Release 50BF_K12	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

5.10 Tiempo Actuación 87L_ Falla L3:

Test Settings

State	Pre-Falla	Falla Fase L3	Post-Falla
I L1	100,0 mA 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	5,000 A 0,00 ° 50,000 Hz
I L2	100,0 mA -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	5,000 A -120,00 ° 50,000 Hz

I L3	100,0 mA 120,00 ° 50,000 Hz	1,000 A 120,00 ° 50,000 Hz	5,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 19:40:08	Test End:	11-abr.-2019 19:40:13
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Tiempo_87L	Falla Fase L3	Falla Fase L3	TRIP-L1_K11 0>1	30,00 ms	20,00 ms	20,00 ms	37,10 ms	7,100 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

5.11 Tiempo Actuación 87L_ Falla L1-L2-L3:

Test Settings

State	Pre-Falla	Falla Trifasica	Post-Falla
I L1	100,0 mA 0,00 ° 50,000 Hz	1,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	100,0 mA -120,00 ° 50,000 Hz	1,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	100,0 mA 120,00 ° 50,000 Hz	1,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 19:42:43	Test End:	11-abr.-2019 19:42:49
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Tiempo_87L	Falla Trifasica	Falla Trifasica	TRIP-L1_K11 0>1	30,00 ms	20,00 ms	20,00 ms	42,50 ms	12,50 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

5.12 Falla 87L_ START 50BF:

Test Settings

State	Pre-Falla	Falla Trifasica	Post-Falla
I L1	100,0 mA 0,00 ° 50,000 Hz	1,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	100,0 mA -120,00 ° 50,000 Hz	1,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	100,0 mA 120,00 ° 50,000 Hz	1,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	11-abr.-2019 19:55:45	Test End:	11-abr.-2019 19:55:49
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
START_50BFK11	Falla Trifasica	Falla Trifasica	Release 50BF_K11 0>1	30,00 ms	20,00 ms	20,00 ms	44,50 ms	14,50 ms	+
RELEASE K11	Falla Trifasica	Falla Trifasica	Start_50BF K11 0>1	30,00 ms	20,00 ms	20,00 ms	45,90 ms	15,90 ms	+
START_50BFK12	Falla Trifasica	Falla Trifasica	Release 50BF_K12 0>1	30,00 ms	20,00 ms	20,00 ms	43,80 ms	13,80 ms	+
RELEASE K12	Falla Trifasica	Falla Trifasica	Start_50BF K12 0>1	30,00 ms	20,00 ms	20,00 ms	43,80 ms	13,80 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Pre-Falla	Falla Trifasica	Post-Falla
Assess	+	+	+
Tolerance	0,000 s	200,0 ms	200,0 ms

TRIP-L2_K11	0	1	0
TRIP-L3_K11	0	1	0
TRIP-L1_K12	0	1	0
TRIP-L2_K12	0	1	0
TRIP-L3_K12	0	1	0
Start_50BF K11	0	1	0
Release 50BF_K11	0	1	0
Start_50BF K12	0	1	0
Release 50BF_K12	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

Release 50BF_K9

Group end:5.- Arranque 87L