ARCHIVO DE PRUEBAS
OMICRON

AUDITORIA TECNICA DE EQUIPOS DE PROTECCIONES.

PROTECCION DE FALLA INTERRUPTOR 52J14 EN S/E MAITENCILLO MODELO 7VK87, MARCA SIEMENS, TECNOLOGIA SIPROTEC 5

INGEMA S. A	**CLIENTE**

Test Object - Device Settings

Substation/Bay:

Substation:	CARDONES 500 kV	Substation address:	COPIAPO
Bay:	J14	Bay address:	

Device:

Name/description:	J14_R01_F007	Manufacturer:	SIEMENS
Device type:	7VK87	Device address:	P1D8321
Serial/model number:	7VK87-DAAA-AA0-0AAAA0-AC0111-12111B-BAA000-000AA0-CH1BA1-CG0		
Additional info 1:	50BF_PAÑO J14		
Additional info 2:			

Hardware

Test Equipment

Type	Serial Number
CMC356	HE295P

Hardware Check

Performed At	Result	Details
04-04-2019 10:30:51	Passed	

Group:1. Verificacion Medida Fase L1

1.1 Inyeccion 25% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:37:14	Test End:	04-abr.-2019 10:39:19
User Name:		Manager:	
Company:			

Test Results

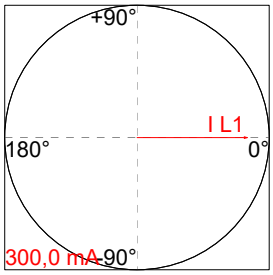
Title: Verificacion de Medida al 25% Fase A

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	250,0 mA	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,250A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed

Online access ▸ SIPROTEC 5 devices connected via USB ▸ 7VK87 (Assigned) ▸ Measurements ▸

Snapshot Reset Show values as: primary CSV

The values are displayed from normal operation. Set/reset of statistics, functional and user-defined values is allowed.

Fundamental | Function values | Statistics | User-def. values

Measurements	Value	Quality	Number
Fundamental			
Vph:A	0 kV, ∠0 °	good (process)	301.1501.10391.302
Vph:B	0 kV, ∠0 °	good (process)	301.1501.10391.302
Vph:C	0 kV, ∠0 °	good (process)	301.1501.10391.302
Vpp:AB	0 kV, ∠0 °	good (process)	301.1501.10391.301
Vpp:BC	0 kV, ∠0 °	good (process)	301.1501.10391.301
Vpp:CA	0 kV, ∠0 °	good (process)	301.1501.10391.301
Iph:A	500 A, ∠0 °	good (process)	301.1501.10391.300
Iph:B	0 A, ∠0 °	good (process)	301.1501.10391.300
Iph:C	0 A, ∠0 °	good (process)	301.1501.10391.300
IN	501 A, ∠-180 °	good (process)	301.1501.10391.303

1.2 Inyeccion 50% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:39:24	Test End:	04-abr.-2019 10:40:04
User Name:		Manager:	
Company:			

Test Results

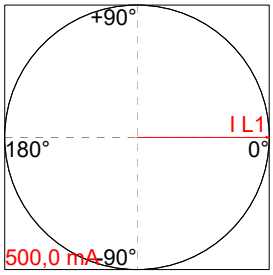
Title: Verificacion de Medida Fase A al 50%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	500,0 mA	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,500A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



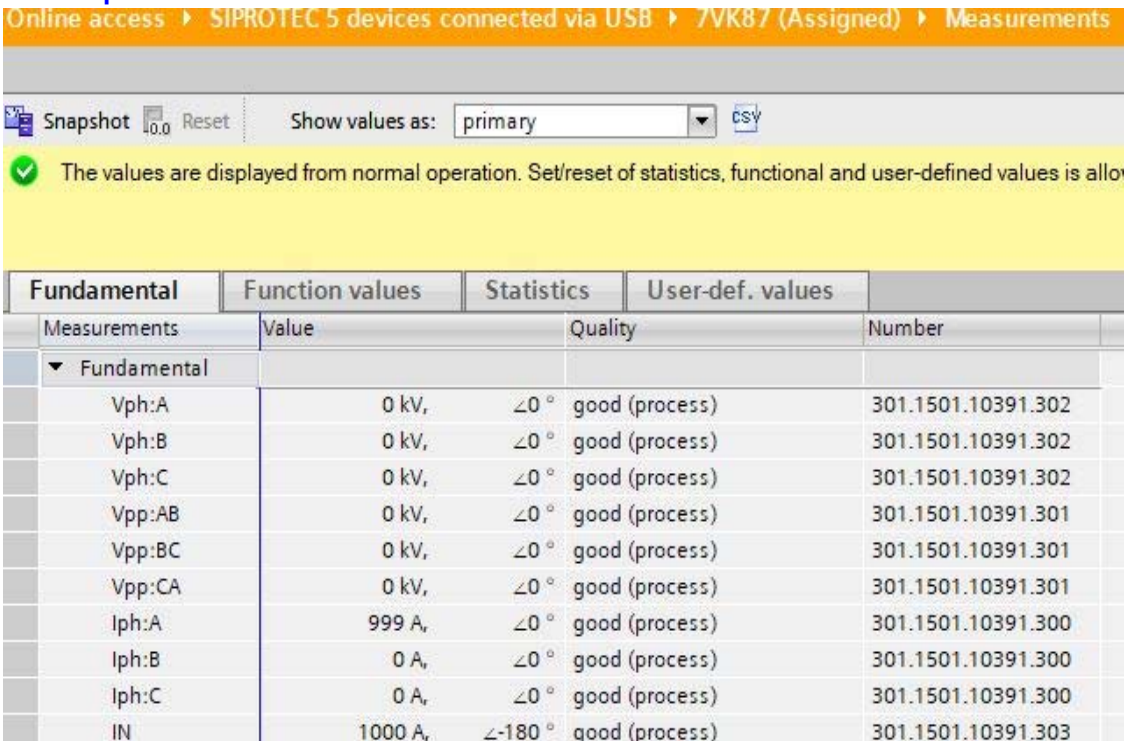
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:40:37	Test End:	04-abr.-2019 10:41:10
User Name:		Manager:	
Company:			

Test Results

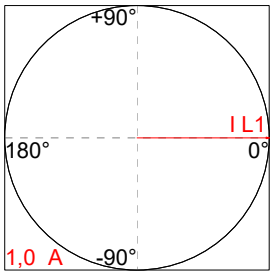
Title: Verificacion Medida Fase A al 100%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	1,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	1,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



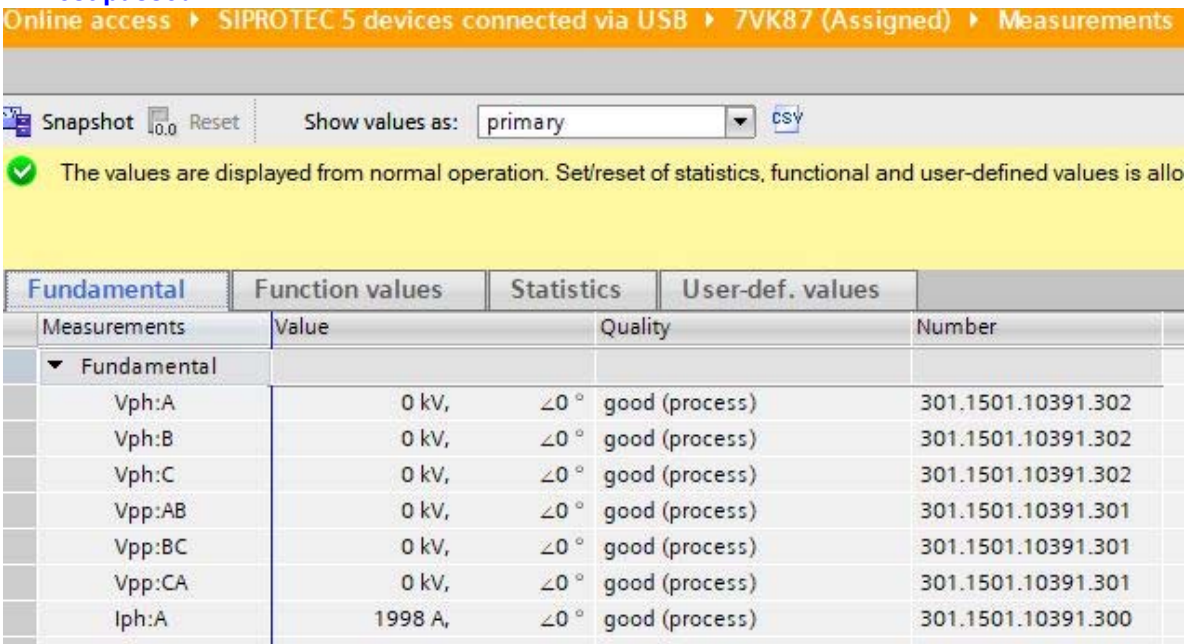
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
DSIP.L2_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Measurements	Value		Quality	Number
Fundamental				
Vph:A	0 kV,	∠0 °	good (process)	301.1501.10391.302
Vph:B	0 kV,	∠0 °	good (process)	301.1501.10391.302
Vph:C	0 kV,	∠0 °	good (process)	301.1501.10391.302
Vpp:AB	0 kV,	∠0 °	good (process)	301.1501.10391.301
Vpp:BC	0 kV,	∠0 °	good (process)	301.1501.10391.301
Vpp:CA	0 kV,	∠0 °	good (process)	301.1501.10391.301
Iph:A	1998 A,	∠0 °	good (process)	301.1501.10391.300

Group end:1. Verificacion Medida Fase L1

Group:2. Verificacion Medida Fase L2

2.1 Inyeccion 25% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:41:19	Test End:	04-abr.-2019 10:41:56
User Name:		Manager:	
Company:			

Test Results

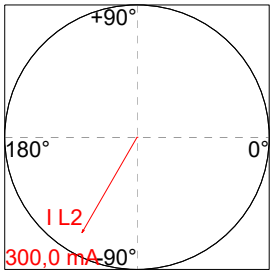
Title: Verificacion de Medida Fase B al 25%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	250,0 mA	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,250A	-120,00°
I L3	0,000A	120,00°



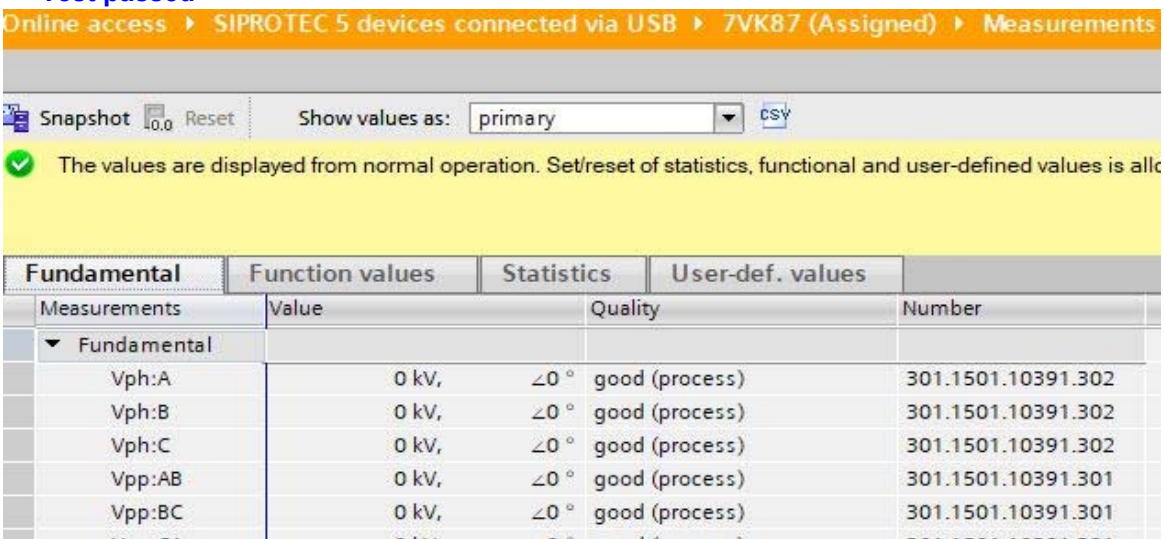
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



2.2 Inyeccion 50% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:42:02	Test End:	04-abr.-2019 10:42:42
User Name:		Manager:	
Company:			

Test Results

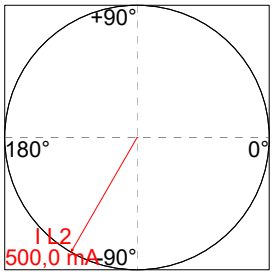
Title: Verificacion de Medida Fase B al 50%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	500,0 mA	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,500A	-120,00°
I L3	0,000A	120,00°



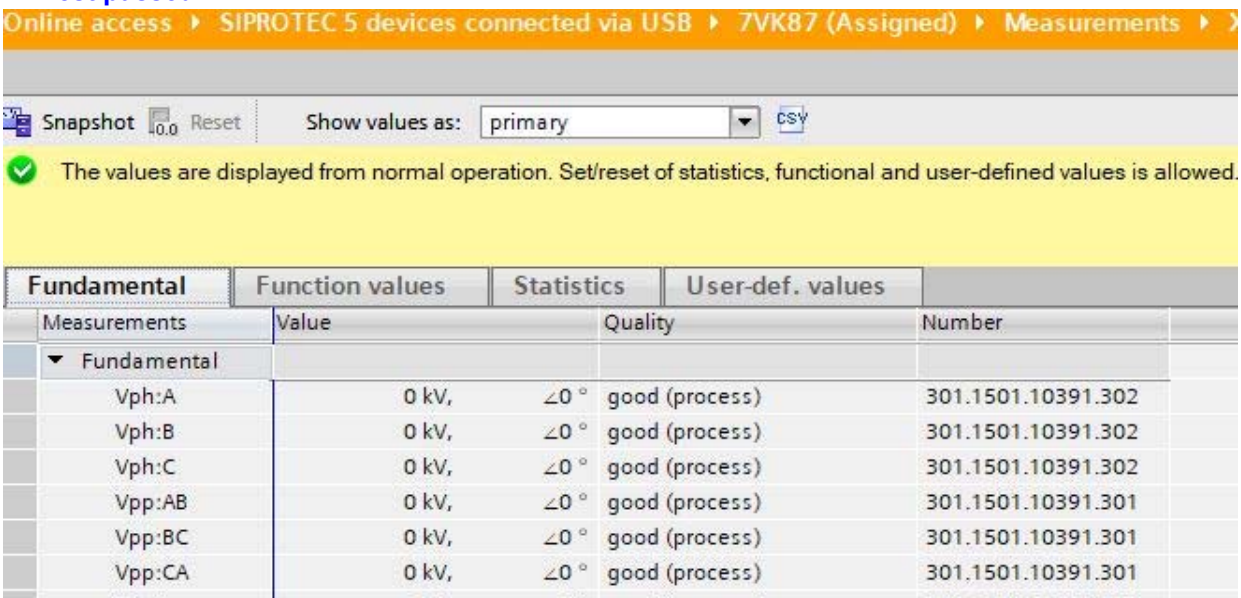
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



2.3 Inyeccion 100% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:42:49	Test End:	04-abr.-2019 10:43:23
User Name:		Manager:	
Company:			

Test Results

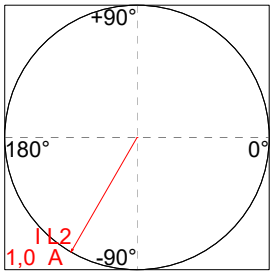
Title: Verificacion de Medida Fase B al 100%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	1,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	1,000A	-120,00°
I L3	0,000A	120,00°



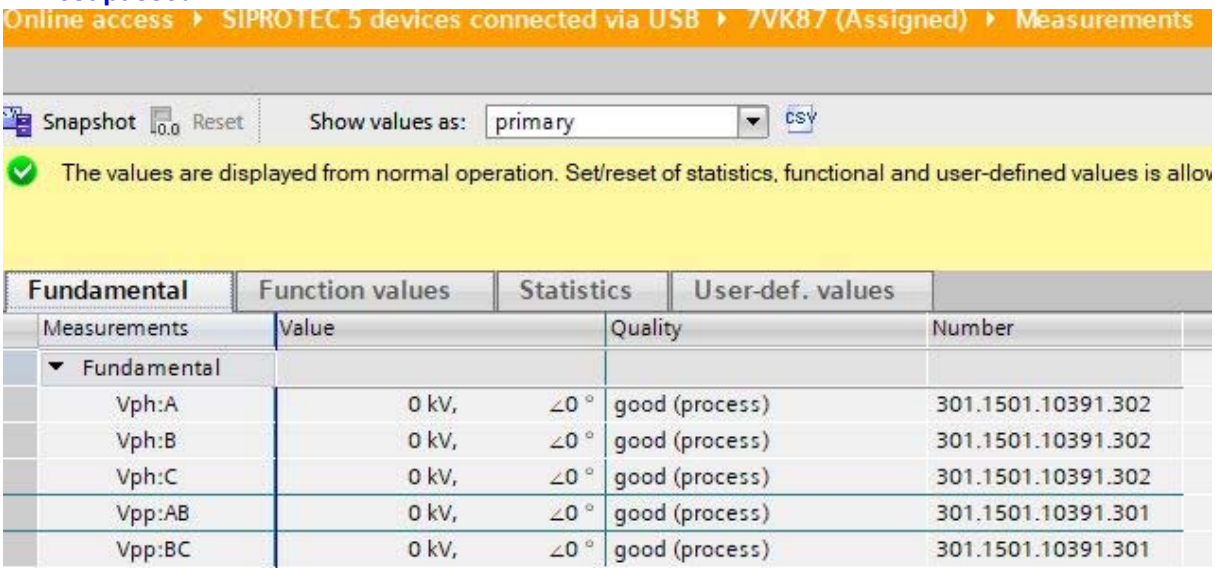
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:2. Verificacion Medida Fase L2

Group:3. Verificacion Medida Fase L3

3.1 Inyeccion 25% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:43:30	Test End:	04-abr.-2019 10:44:25
User Name:		Manager:	
Company:			

Test Results

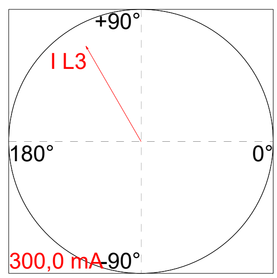
Title: Verificacion de Medida Fase C al 25%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	250,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,250A	120,00°



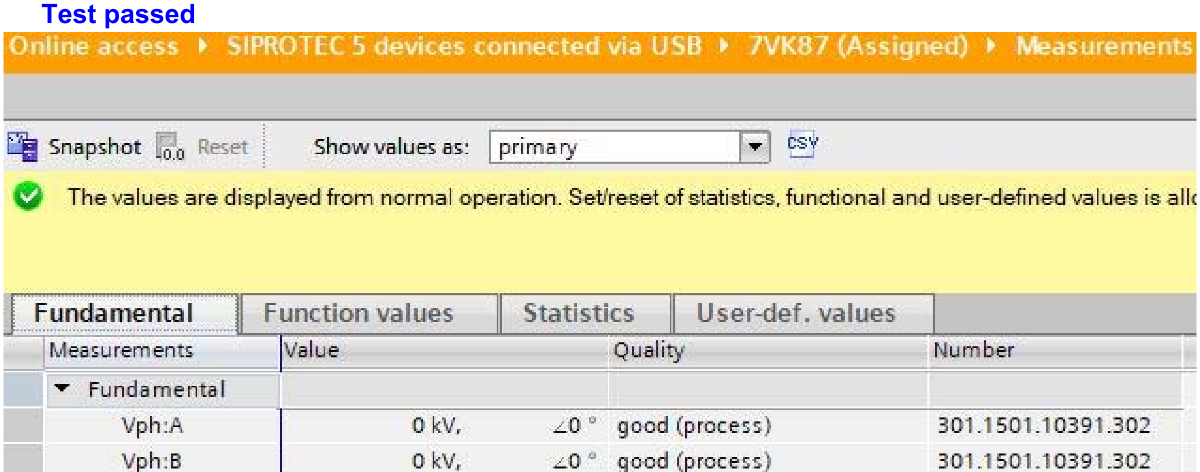
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed   100,00% passed

Test passed



Measurements	Value		Quality	Number
Fundamental				
Vph:A	0 kV,	∠0 °	good (process)	301.1501.10391.302
Vph:B	0 kV,	∠0 °	good (process)	301.1501.10391.302

3.2 Inyeccion 50% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:45:00	Test End:	04-abr.-2019 10:45:41
User Name:		Manager:	
Company:			

Test Results

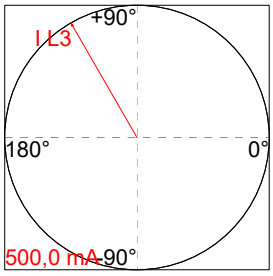
Title: Verificacion Medida Fase C al 50%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	500,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,500A	120,00°



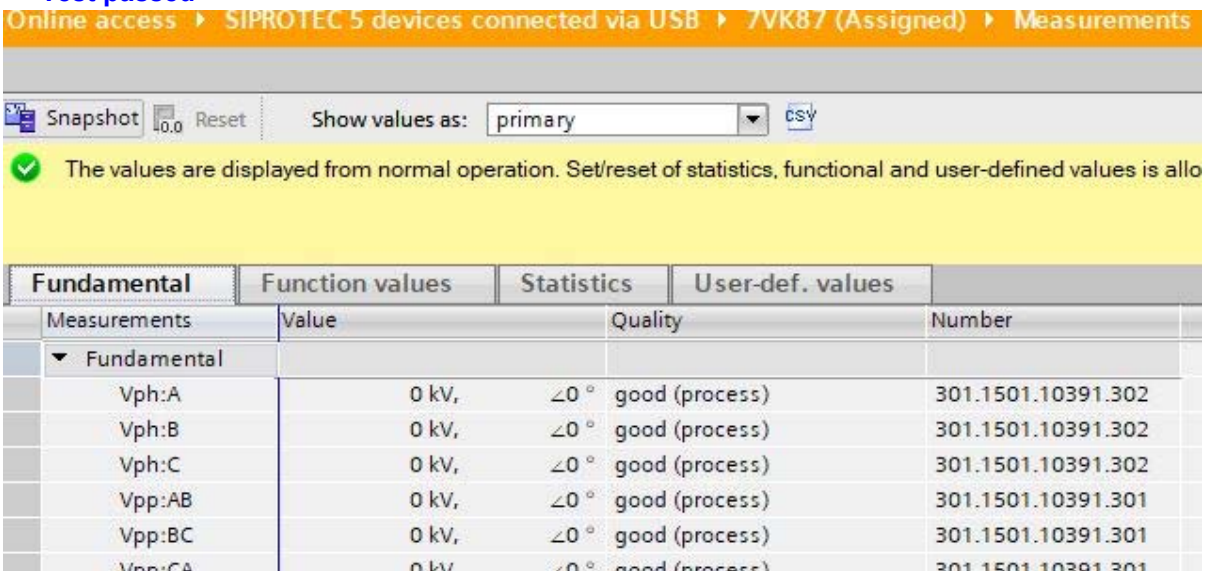
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
DSIP.L2_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



3.3 Inyeccion 100% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:46:16	Test End:	04-abr.-2019 10:46:51
User Name:		Manager:	
Company:			

Test Results

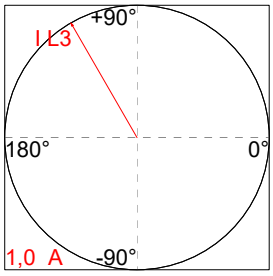
Title: Verificacion Msedida Fase C al 100%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	1,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	1,000A	120,00°



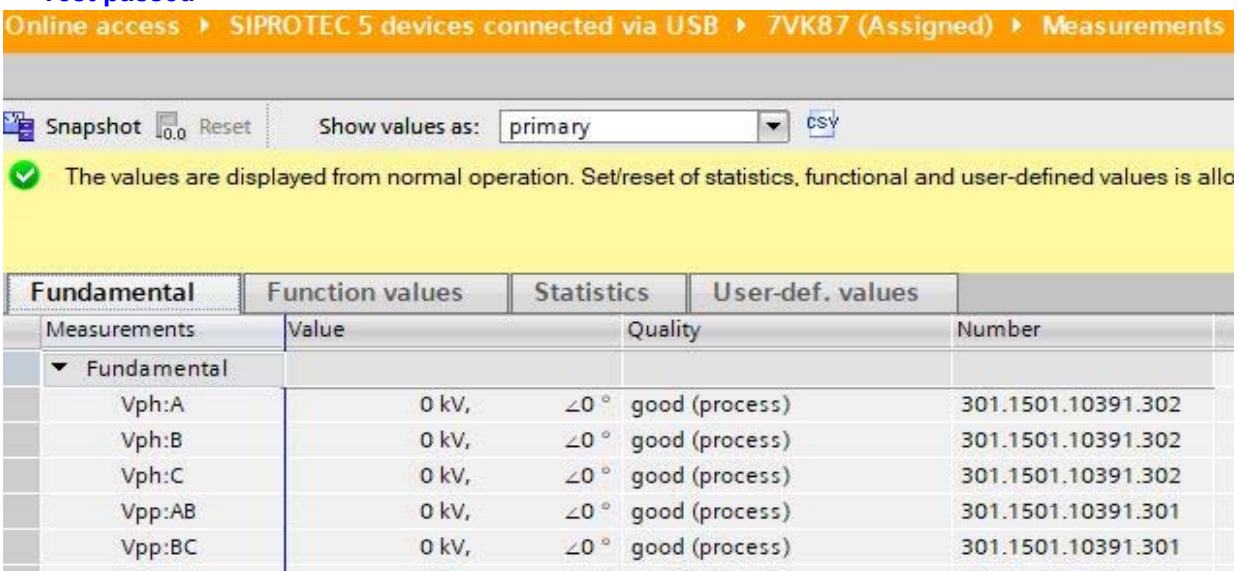
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
DSIP.L2_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:3. Verificacion Medida Fase L3

Group:4. Verificacion Medida Fases L123

4.1 Inyeccion 25% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:47:21	Test End:	04-abr.-2019 10:48:01
User Name:		Manager:	
Company:			

Test Results

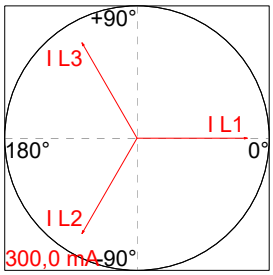
Title: Verificacion Medida Fases ABC al 25%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	250,0 mA	0,00 °	50,000 Hz
	I L2	250,0 mA	-120,00 °	50,000 Hz
	I L3	250,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,250A	0,00°
I L2	0,250A	-120,00°
I L3	0,250A	120,00°



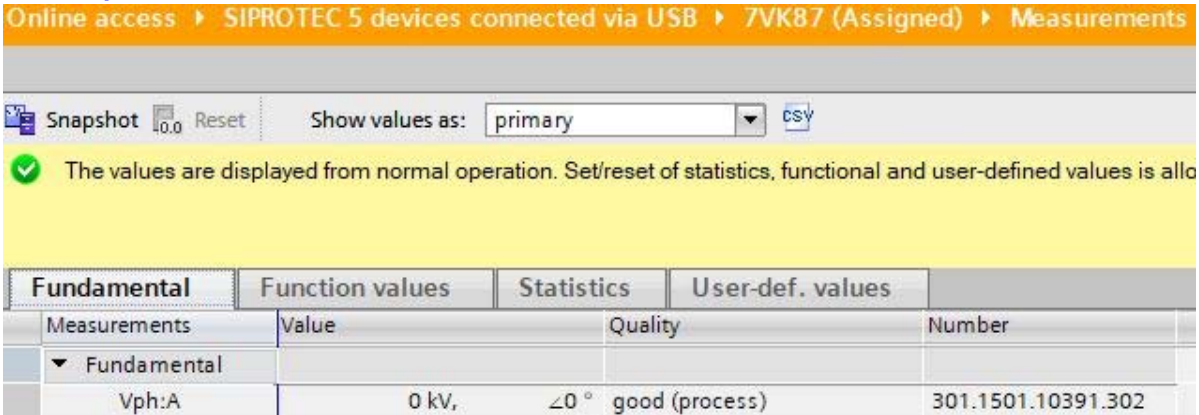
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
DSIP.L2_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



4.2 Inyeccion 50% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:48:23	Test End:	04-abr.-2019 10:48:54
User Name:		Manager:	
Company:			

Test Results

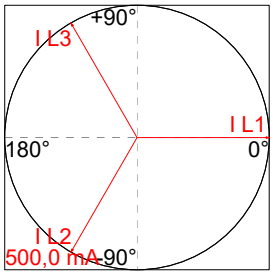
Title: Verificacion Medida Fases ABC al 50%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	500,0 mA	0,00 °	50,000 Hz
	I L2	500,0 mA	-120,00 °	50,000 Hz
	I L3	500,0 mA	120,00 °	50,000 Hz

Generator Settings

I L1	0,500A	0,00°
I L2	0,500A	-120,00°
I L3	0,500A	120,00°



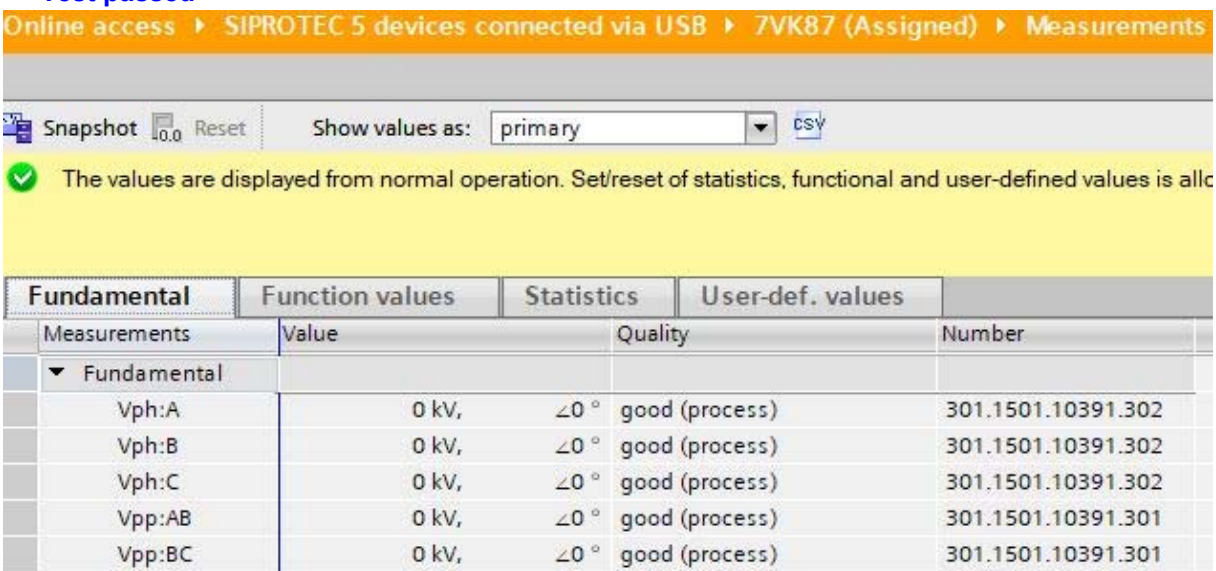
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
DSIP.L2_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



4.3 Inyeccion 100% de Inominal:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 10:49:18	Test End:	04-abr.-2019 10:50:04
User Name:		Manager:	
Company:			

Test Results

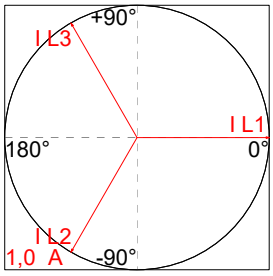
Title: Verifiacion Medida Fases ABC al 100%

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	1,000 A	0,00 °	50,000 Hz
	I L2	1,000 A	-120,00 °	50,000 Hz
	I L3	1,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	1,000A	0,00°
I L2	1,000A	-120,00°
I L3	1,000A	120,00°



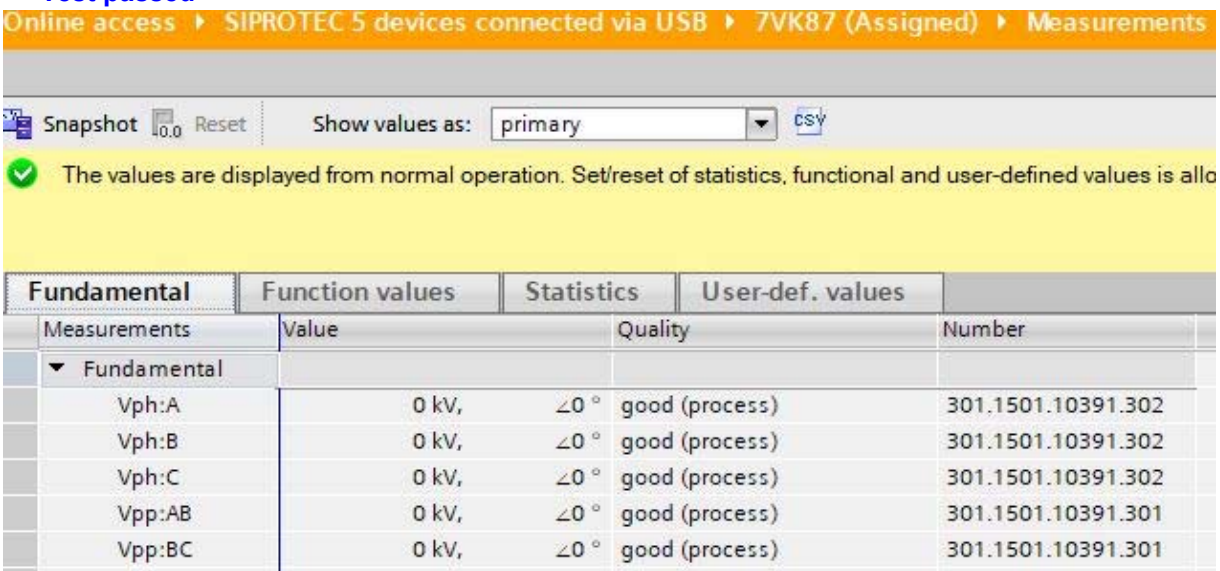
Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
DSIP.L2_52J14 BOB2	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed



Group end:4. Verificacion Medida Fases L123

Group:5. Verificacion Pickup 50BF Fase L1

5.1 Pickup con Arranque Fase L1:

Test Settings

General

No. of ramp states: 1
Total steps per test: 101
Total time per test: 5,050 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	1,200 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	1,200 A
Sig 1 To	1,300 A
Sig 1 Delta	1,000 mA
Sig 1 d/dt	20,00 mA/s
ARRANQ_L1	1
ARRANQ. L2	0
ARRANQ. L3	0
ARRANQ. L1L2L3	0
dt per Step	50,00 ms
Ramp Steps	101
Ramp Time	5,050s
Trigger	Bin
Trigger Logic	OR
DISP. L1_52J14	1
DISP. L2_52J14	X
DISP.L3_52J14	X
ENVIO DDT	X
DISP. 50BF_ET2/0	X
DSIP.L1_52J14 BOB2	X
DSIP.L2_52J14 BOB2	X
Step back	No
Delay Time	100,0 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	04-abr.-2019 11:09:12	Test End:	04-abr.-2019 11:09:15
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup 50BF_ L1	Ramp 1	DISP. L1_52J14 0->1	I L1	1,200 A	1,203 A	300,0 mA	300,0 mA	3,000 mA	+	17,80 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

5.2 Pickup sin Arranque Fase L1:

Test Settings

General

No. of ramp states:	1
Total steps per test:	101
Total time per test:	30,300 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	1,200 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From **Sig 1 To** **Sig 1 Delta** **Sig 1 d/dt**	1,200 A 1,300 A 1,000 mA 3,333 mA/s
ARRANQ_L1 **ARRANQ. L2** **ARRANQ. L3** **ARRANQ. L1L2L3**	0 0 0 0
dt per Step **Ramp Steps** **Ramp Time**	300,0 ms 101 30,300s
Trigger	Bin
Trigger Logic **DISP. L1_52J14**	OR 1

DISP. L2_52J14	X
DISP.L3_52J14	X
ENVIO DDT	X
DISP. 50BF_ET2/0	X
DSIP.L1_52J14 BOB2	X
DSIP.L2_52J14 BOB2	X
Step back	Yes
Delay Time	100,0 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	04-abr.-2019 11:11:19	Test End:	04-abr.-2019 11:11:51
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

Group end:5. Verificacion Pickup 50BF Fase L1

Group:6. Verificacion Pickup 50BF Fase L2

6.1 Pickup con Arranque Fase L2:

Test Settings

General

No. of ramp states:	1
Total steps per test:	101
Total time per test:	10,100 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	1,200 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	1,200 A

Sig 1 To	1,300 A
Sig 1 Delta	1,000 mA
Sig 1 d/dt	10,00 mA/s
ARRANQ_L1	0
ARRANQ. L2	1
ARRANQ. L3	0
ARRANQ. L1L2L3	0
dt per Step	100,0 ms
Ramp Steps	101
Ramp Time	10,100s
Trigger	Bin
Trigger Logic	OR
DISP. L1_52J14	X
DISP. L2_52J14	1
DISP.L3_52J14	X
ENVIO DDT	X
DISP. 50BF_ET2/0	X
DSIP.L1_52J14 BOB2	X
DSIP.L2_52J14 BOB2	X
Step back	Yes
Delay Time	20,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	04-abr.-2019 11:15:17	Test End:	04-abr.-2019 11:15:20
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	DISP. L2_52J14 0->1	I L2	1,200 A	1,202 A	300,0 mA	300,0 mA	2,000 mA	+	74,00 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

6.2 Pickup sin Arranque Fase L2:

Test Settings

General

No. of ramp states:	1
Total steps per test:	101
Total time per test:	10,100 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	1,200 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	1,200 A
Sig 1 To	1,300 A
Sig 1 Delta	1,000 mA
Sig 1 d/dt	10,00 mA/s
ARRANQ_L1	0
ARRANQ. L2	0
ARRANQ. L3	0
ARRANQ. L1L2L3	0
dt per Step	100,0 ms
Ramp Steps	101
Ramp Time	10,100s
Trigger	Bin
Trigger Logic	OR
DISP. L1_52J14	X
DISP. L2_52J14	1
DISP.L3_52J14	X
ENVIO DDT	X
DISP. 50BF_ET2/0	X
DSIP.L1_52J14 BOB2	X
DSIP.L2_52J14 BOB2	X
Step back	No
Delay Time	0,000 s

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	04-abr.-2019 11:16:49	Test End:	04-abr.-2019 11:17:02
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

Group end:6. Verificacion Pickup 50BF Fase L2

Group:7. Verificacion Pickup 50BF Fase L3

7.1 Pickup con Arranque Fase L3:

Test Settings

General

No. of ramp states:	1
Total steps per test:	21
Total time per test:	2,100 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	1,200 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	1,200 A
Sig 1 To	1,300 A
Sig 1 Delta	5,000 mA
Sig 1 d/dt	50,00 mA/s
ARRANQ_L1	0
ARRANQ. L2	0
ARRANQ. L3	1
ARRANQ. L1L2L3	0
dt per Step	100,0 ms
Ramp Steps	21
Ramp Time	2,100s
Trigger	Bin
Trigger Logic	OR
DISP. L1_52J14	X
DISP. L2_52J14	X
DISP.L3_52J14	1
ENVIO DDT	X
DISP. 50BF_ET2/0	X
DSIP.L1_52J14 BOB2	X
DSIP.L2_52J14 BOB2	X
Step back	Yes
Delay Time	20,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	04-abr.-2019 11:21:07	Test End:	04-abr.-2019 11:21:10
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	DISP.L3_52 J14 0->1	I L3	1,200 A	1,205 A	300,0 mA	300,0 mA	5,000 mA	+	70,10 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

7.2 Pickup sin Arranque Fase L3:

Test Settings

General

No. of ramp states: 1
Total steps per test: 101
Total time per test: 10,100 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	1,200 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From **Sig 1 To** **Sig 1 Delta** **Sig 1 d/dt**	1,200 A 1,300 A 1,000 mA 10,00 mA/s
ARRANQ_L1 **ARRANQ. L2** **ARRANQ. L3** **ARRANQ. L1L2L3**	0 0 0 0
dt per Step **Ramp Steps** **Ramp Time**	100,0 ms 101 10,100s
Trigger	Bin
Trigger Logic **DISP. L1_52J14** **DISP. L2_52J14** **DISP.L3_52J14** **ENVIO DDT** **DISP. 50BF_ET2/0** **DSIP.L1_52J14 BOB2**	OR X X 1 X X X
Step back	No

Delay Time	0,000 s

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	04-abr.-2019 11:22:01	Test End:	04-abr.-2019 11:22:13
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

Group end:7. Verificacion Pickup 50BF Fase L3

Group:8. Verificacion Pickup 50BF Fases L123

8.1 Pickup con Arranque Fases L123:

Test Settings

General

No. of ramp states:	1
Total steps per test:	101
Total time per test:	10,100 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	1,200 A 0,00 ° 50,000 Hz
I L2	1,200 A -120,00 ° 50,000 Hz
I L3	1,200 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	1,200 A
Sig 1 To	1,300 A
Sig 1 Delta	1,000 mA
Sig 1 d/dt	10,00 mA/s
ARRANQ_L1	0
ARRANQ. L2	0
ARRANQ. L3	0
ARRANQ. L1L2L3	1
dt per Step	100,0 ms
Ramp Steps	101
Ramp Time	10,100s
Trigger	Bin
Trigger Logic	AND

DISP. L1_52J14	1
DISP. L2_52J14	1
DISP.L3_52J14	1
ENVIO DDT	X
DISP. 50BF_ET2/0	X
DSIP.L1_52J14 BOB2	X
DSIP.L2_52J14 BOB2	X
Step back	Yes
Delay Time	20,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	04-abr.-2019 11:25:40	Test End:	04-abr.-2019 11:25:42
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L123	Ramp 1	DISP.L3_52 J14 0->1 and DISP. L1_52J14 0->1 and DISP. L2_52J14 0->1	I L1; L2; L3	1,200 A	1,201 A	300,0 mA	300,0 mA	1,000 mA	+	88,20 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

8.2 Pickup sin Arranque Fases L123:

Test Settings

General

No. of ramp states:	1
Total steps per test:	101
Total time per test:	10,100 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	1,200 A 0,00 ° 50,000 Hz
I L2	1,200 A -120,00 ° 50,000 Hz
I L3	1,200 A 120,00 ° 50,000 Hz

Force abs. Phases	No
Sig 1 From	1,200 A
Sig 1 To	1,300 A
Sig 1 Delta	1,000 mA
Sig 1 d/dt	10,00 mA/s
ARRANQ_L1	0
ARRANQ. L2	0
ARRANQ. L3	0
ARRANQ. L1L2L3	0
dt per Step	100,0 ms
Ramp Steps	101
Ramp Time	10,100s
Trigger	Bin
Trigger Logic	OR
DISP. L1_52J14	1
DISP. L2_52J14	1
DISP.L3_52J14	1
ENVIO DDT	X
DISP. 50BF_ET2/0	X
Step back	No
Delay Time	0,000 s

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	04-abr.-2019 11:26:18	Test End:	04-abr.-2019 11:26:30
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

8.3 No operacion con Contacto CB:

Test Module

Name:	OMICRON QuickCMC	Version:	4.00
Test Start:	04-abr.-2019 11:28:18	Test End:	04-abr.-2019 11:30:11
User Name:		Manager:	
Company:			

Test Results

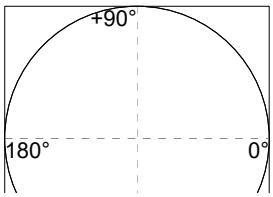
Title: Verificacion No operacion con Arranque sin Corriente (CB Close)

Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	I L1	0,000 A	0,00 °	50,000 Hz
	I L2	0,000 A	-120,00 °	50,000 Hz
	I L3	0,000 A	120,00 °	50,000 Hz

Generator Settings

I L1	0,000A	0,00°
I L2	0,000A	-120,00°
I L3	0,000A	120,00°



Binary Inputs

Name	Slope	Time
DISP. L1_52J14	0	
DISP. L2_52J14	0	
DISP.L3_52J14	0	
ENVIO DDT	0	
DISP. 50BF_ET2/0	0	
DSIP.L1_52J14 BOB2	0	
DSIP.L2_52J14 BOB2	0	
Bin. in 8	0	
Bin. in 9	0	
Bin. in 10	0	
Overload	0	

Summary

1 tests passed, 0 tests failed, 0 tests not assessed 100,00% passed

Test passed

Group end:8. Verificacion Pickup 50BF Fases L123

Group:9. Operacion 50BF_K2 (T1)

9.1 Operacion 50BF_Fase L1 :

Test Settings

State	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1	Post-Falla 3
I L1	800,0 mA 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 11:31:30	Test End:	04-abr.-2019 11:31:39
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL1+C/Arranque 50BF_L1	Pickup IL1+C/Arranque 50BF_L1	DISP. L1_52J14 0>1	50,00 ms	30,00 ms	30,00 ms	78,30 ms	28,30 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

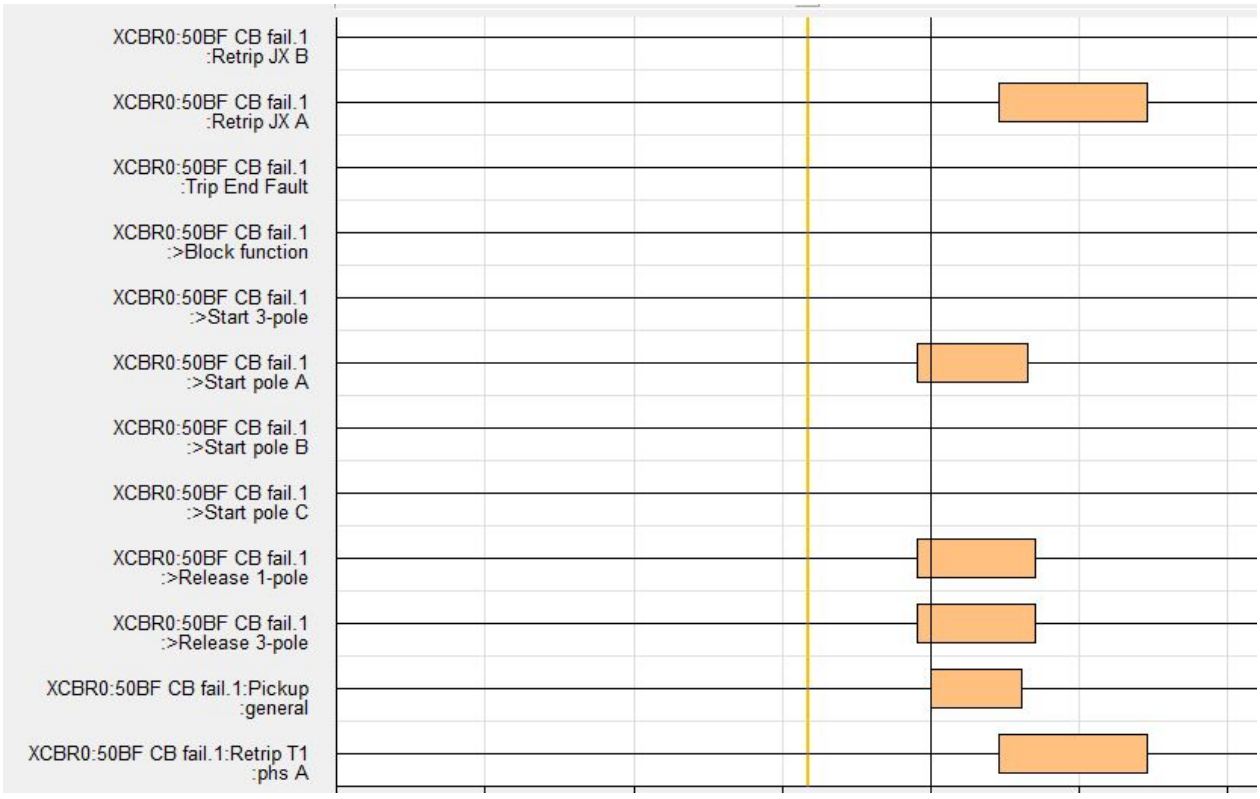
State Assessment

	Prefalla	Pickup IL1+S/Arranque 50BF	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1	Post-Falla 3
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	200,0 ms
DISP. L1_52J14	0	0	0	1	0
DISP. L2_52J14	0	0	0	0	0
DISP.L3_52J14	0	0	0	0	0
ENVIO DDT	0	0	0	0	0
DISP. 50BF_ET2/0	0	0	0	0	0
DSIP.L1_52J14 BOB2	0	0	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed



9.2 Operacion 50BF_Fase L2 :

Test Settings

State	Prefalla	Pickup IL2+S/Arranque 50BF	Post Falla 1	Pickup IL2+C/Arranque 50BF_L2	Post-Falla 2
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	800,0 mA -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 11:33:42	Test End:	04-abr.-2019 11:33:51
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	DISP. L2_52J14 0>1	50,00 ms	30,00 ms	30,00 ms	77,70 ms	27,70 ms	+

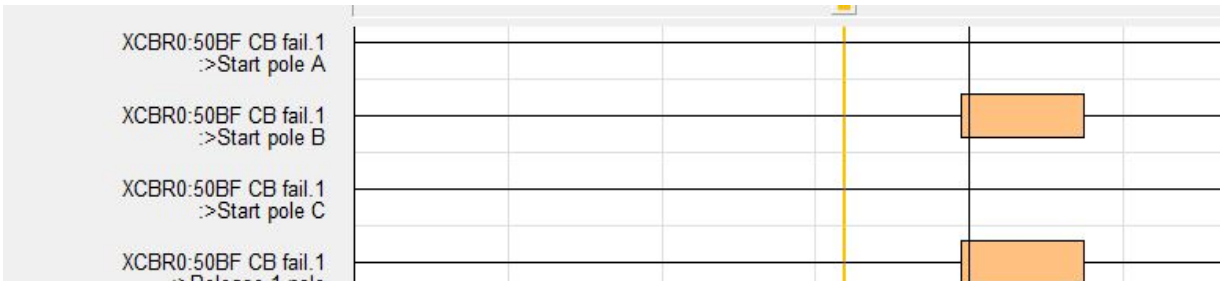
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL2+S/Arranque 50BF	Post Falla 1	Pickup IL2+C/Arranque 50BF_L2	Post-Falla 2
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	200,0 ms
DISP. L1_52J14	0	0	0	0	0
DISP. L2_52J14	0	0	0	1	0
DISP.L3_52J14	0	0	0	0	0
ENVIO DDT	0	0	0	0	0
DISP. 50BF_ET2/0	0	0	0	0	0
DSIP.L1_52J14 BOB2	0	0	0	0	0
DSIP.L2_52J14 BOB2	0	0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed



9.3 Operacion 50BF_Fase L3:

Test Settings

State	Prefalla	Pickup IL3+S/Arranque 50BF	Post Falla 1	Pickup IL3+C/Arranque 50BF_L3	Post-Falla 2
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	800,0 mA 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 11:37:03	Test End:	04-abr.-2019 11:37:10
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL3+C/Arranque 50BF_L3	Pickup IL3+C/Arranque 50BF_L3	DISP.L3_52J14 0>1	50,00 ms	30,00 ms	30,00 ms	76,70 ms	26,70 ms	+

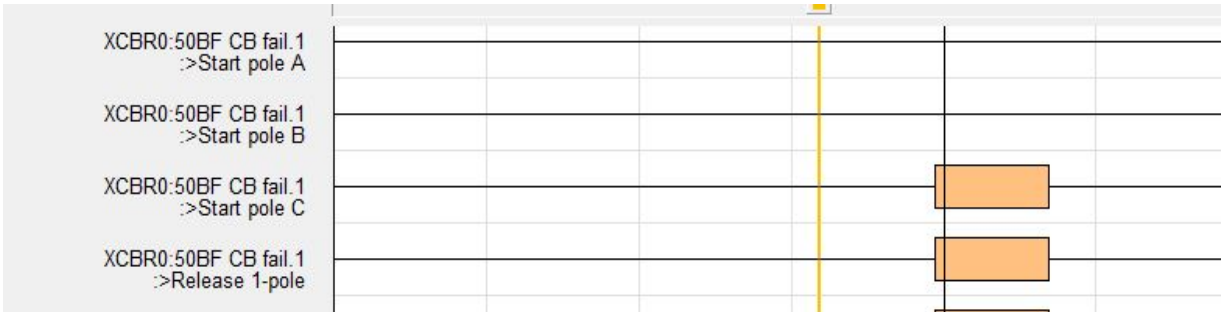
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL3+S/Arranque 50BF	Post Falla 1	Pickup IL3+C/Arranque 50BF_L3	Post-Falla 2
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	200,0 ms
DISP. L1_52J14	0	0	0	1	0
DISP. L2_52J14	0	0	0	0	0
DISP.L3_52J14	0	0	0	0	0
ENVIO DDT	0	0	0	0	0
DISP. 50BF_ET2/0	0	0	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed



9.4 Operacion 50BF_Fase L123:

Test Settings

State	Prefalla	Pickup IL123+S/ Arranque 50BF	Post Falla 1	Pickup IL123+C/ Arranque 50BF_L123	Post-Falla 2
I L1	800,0 mA 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	800,0 mA -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	800,0 mA 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 11:43:55	Test End:	04-abr.-2019 11:44:03
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL123+C/ Arranque 50BF_L123	Pickup IL123+C/ Arranque 50BF_L123	DISP. L2_52J14 0>1	50,00 ms	30,00 ms	30,00 ms	78,60 ms	28,60 ms	+

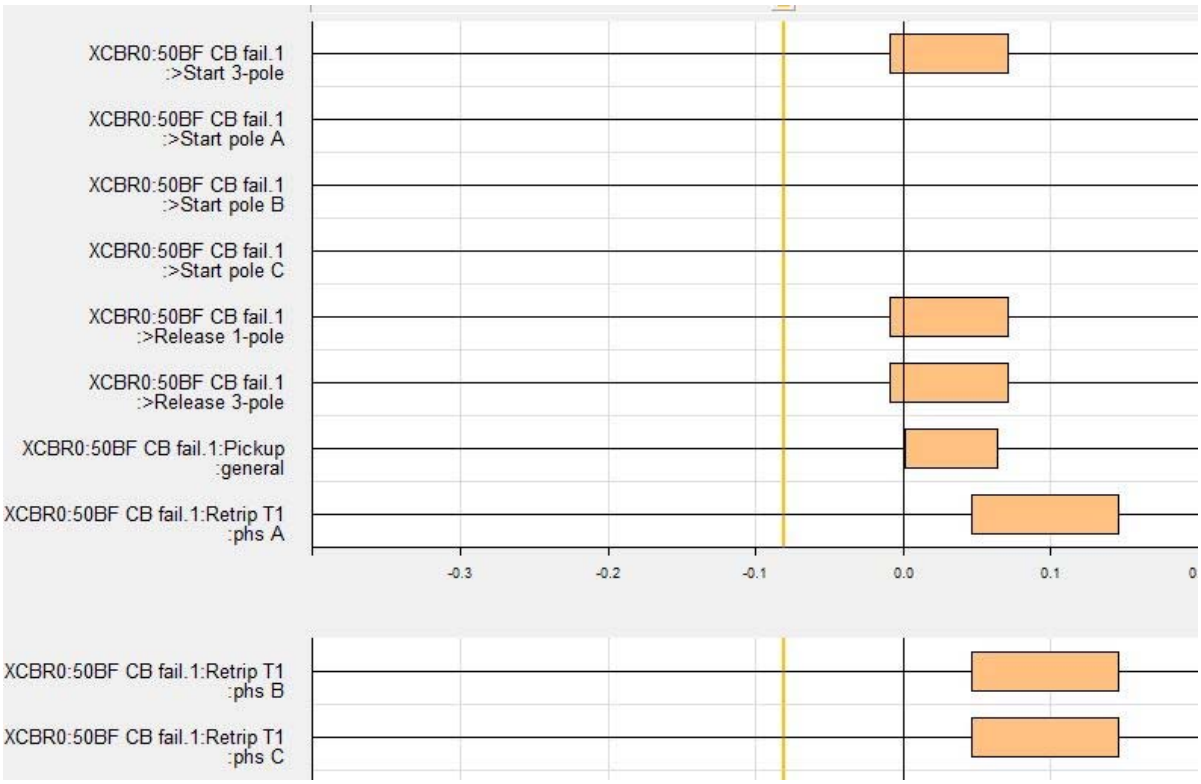
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL123+S/ Arranque 50BF	Post Falla 1	Pickup IL123+C/ Arranque 50BF_L123	Post-Falla 2
Assess	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	200,0 ms
DISP. L1_52J14	0	0	0	1	0
DISP. L2_52J14	0	0	0	1	0
DISP.L3_52J14	0	0	0	1	0
ENVIO DDT	0	0	0	0	0
DISP. 50BF_ET2/0	0	0	0	0	0
DSIP.L1_52J14 BOB2	0	0	0	1	0
DSIP.L2_52J14 BOB2	0	0	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed



Group end:9. Operacion 50BF_K2 (T1)

Group:10. Operacion 50BF_K2 (T1 and T2)

10.1 Operacion 50BF_Fase L1 :

Test Settings

State	Prefalla	Pickup IL1+S/Arranque 50BF_L1	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1 (1)	Pickup IL1+C/Arranque 50BF_L1 (2)	Post-Falla 2
I L1	800,0 mA 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 11:47:47	Test End:	04-abr.-2019 11:47:56
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL1+C/Arranque 50BF_L1 (1)	Pickup IL1+C/Arranque 50BF_L1 (1)	DISP. L1_52J14 0>1	50,00 ms	40,00 ms	40,00 ms	76,50 ms	26,50 ms	+
Disp. 50BF_Etapa 2	Pickup IL1+C/Arranque 50BF_L1 (1)	Pickup IL1+C/Arranque 50BF_L1 (2)	DISP. 50BF_ET 2/0 0>1	220,0 ms	30,00 ms	30,00 ms	225,4 ms	5,400 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

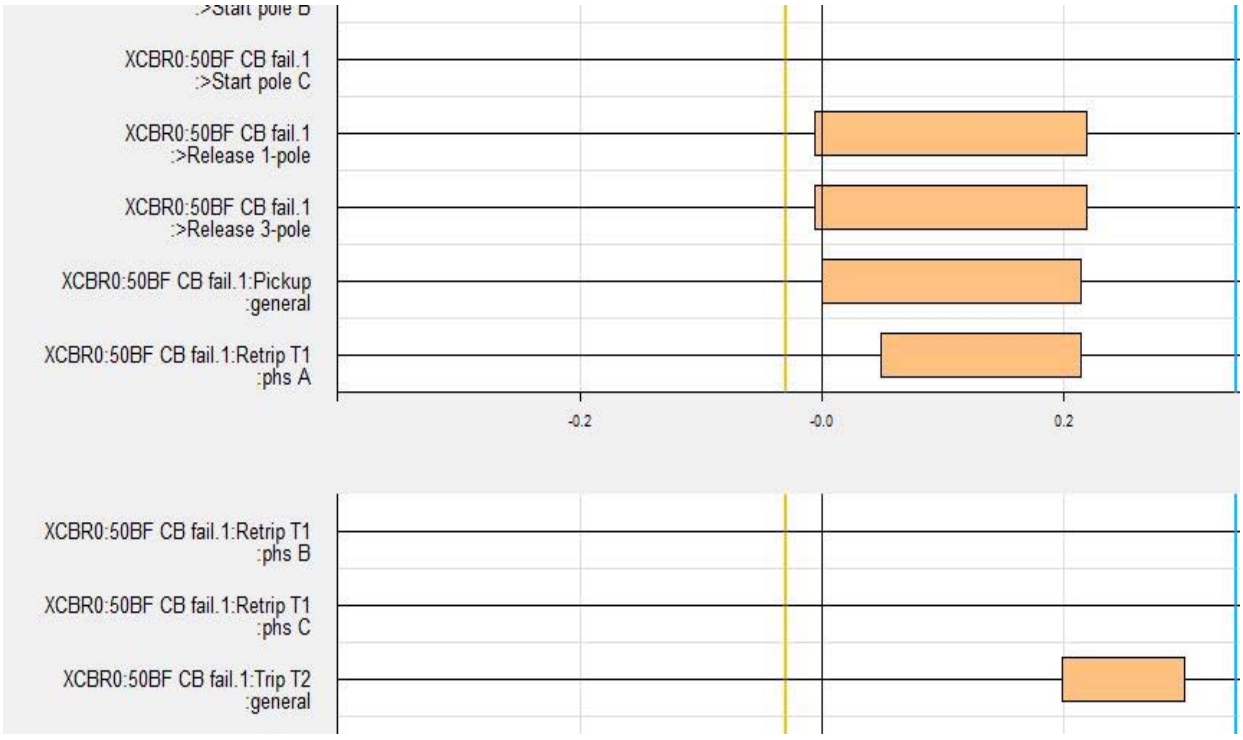
State Assessment

	Prefalla	Pickup IL1+S/Arranque 50BF_L1	Post Falla 1	Pickup IL1+C/Arranque 50BF_L1 (1)	Pickup IL1+C/Arranque 50BF_L1 (2)	Post-Falla 2
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	500,0 ms	200,0 ms
DISP. L1_52J14	0	0	0	1	0	0
DISP. L2_52J14	0	0	0	0	0	0
DISP.L3_52J14	0	0	0	0	0	0
ENVIO DDT	0	0	0	0	1	0
DISP. 50BF_ET2/0	0	0	0	0	1	0
DSIP.L1_52J14 BOB2	0	0	0	0	0	0
DSIP.L2_52J14 BOB2	0	0	0	1	0	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed



10.2 Operacion 50BF_Fase L2:

Test Settings

State	Prefalla	Pickup IL2+S/Arranque 50BF_L2	Post Falla 1	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	Post-Falla 2
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	800,0 mA -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 11:51:21	Test End:	04-abr.-2019 11:51:29
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	DISP. L2_52J14 0>1	50,00 ms	30,00 ms	30,00 ms	78,90 ms	28,90 ms	+
Disp. 50BF_Etapa 2	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	DISP. 50BF_ET 2/0 0>1	200,0 ms	30,00 ms	30,00 ms	228,7 ms	28,70 ms	+

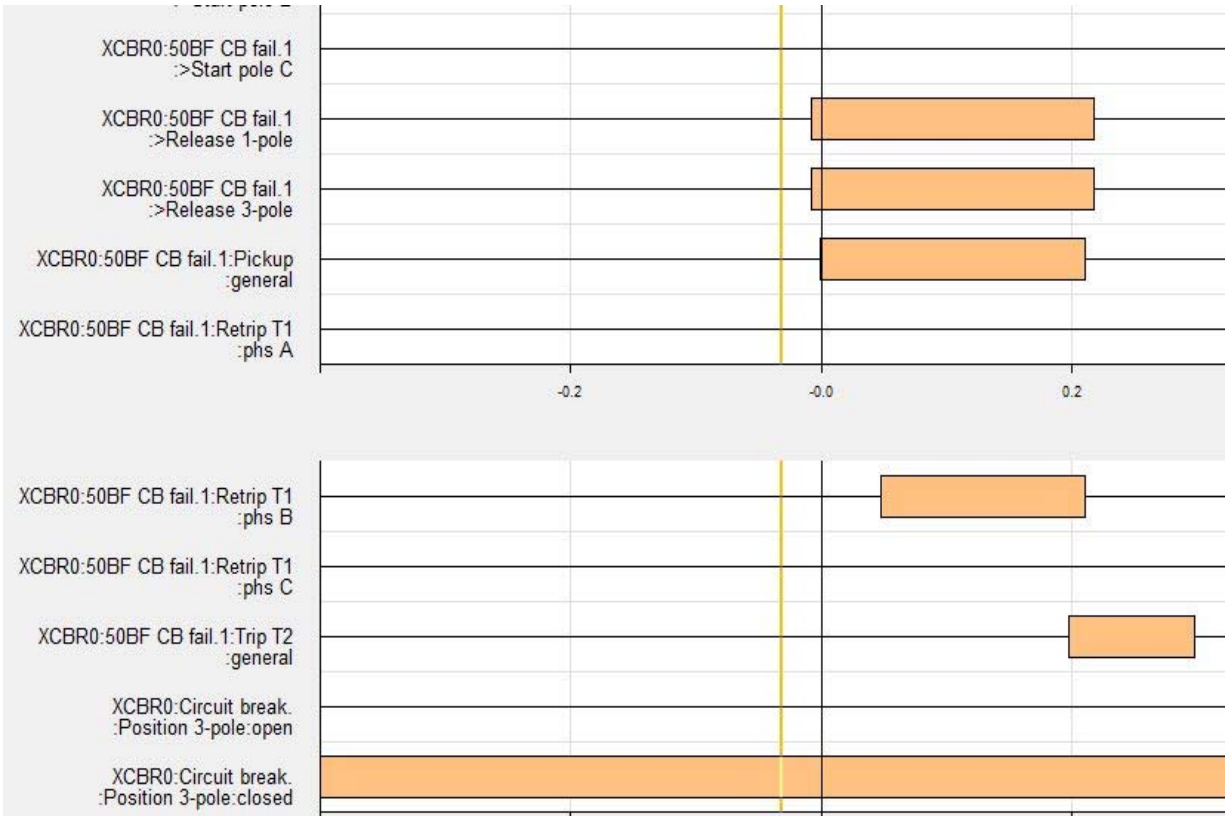
Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Pickup IL2+S/Arranque 50BF_L2	Post Falla 1	Pickup IL2+C/Arranque 50BF_L2	Pickup IL2+C/Arranque 50BF_L2	Post-Falla 2
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	300,0 ms	200,0 ms
DISP. L1_52J14	0	0	0	0	0	0
DISP. L2_52J14	0	0	0	1	0	0
DISP.L3_52J14	0	0	0	0	0	0
ENVIO DDT	0	0	0	0	1	0
DISP. 50BF_ET2/0	0	0	0	0	1	0
DSIP.L1_52J14 BOB2	0	0	0	0	0	0
DSIP.L2_52J14 BOB2	0	0	0	1	0	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed



10.3 Operacion 50BF_Fase L3:

Test Settings

State	Prefalla	Pickup IL3+S/Arranque 50BF_L3	Post Falla 1	Pickup IL3+C/Arranque 50BF_L3	Pickup IL3+C/Arranque 50BF_L3	Post-Falla 3
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	800,0 mA 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 11:52:47	Test End:	04-abr.-2019 11:52:55
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL3+C/Arranque 50BF_L3	Pickup IL3+C/Arranque 50BF_L3	DISP.L3_52J14 0>1	50,00 ms	30,00 ms	30,00 ms	77,80 ms	27,80 ms	+
Disp. 50BF_Etapa 2	Pickup IL3+C/Arranque 50BF_L3	Pickup IL3+C/Arranque 50BF_L3	DISP. 50BF_ET2/0 0>1	200,0 ms	30,00 ms	30,00 ms	226,7 ms	26,70 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

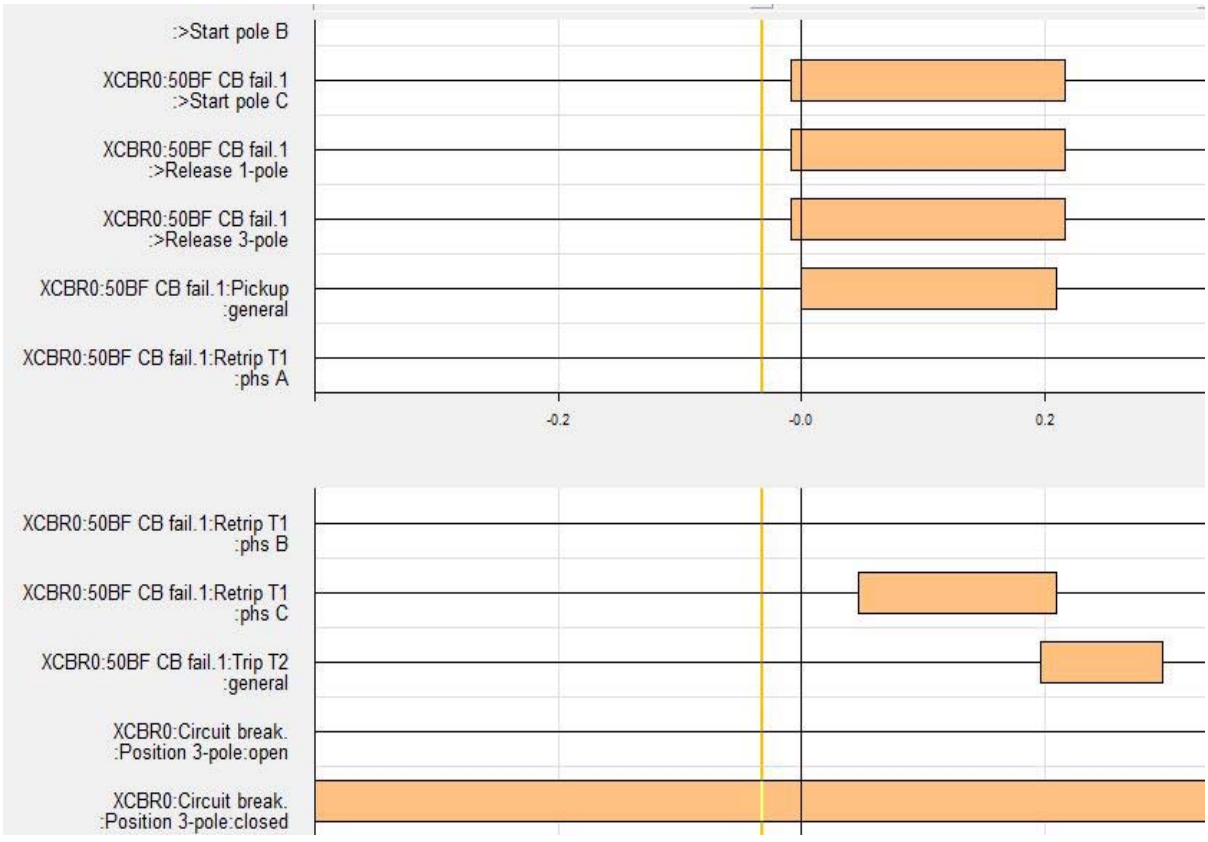
State Assessment

	Prefalla	Pickup IL3+S/Arranque 50BF_L3	Post Falla 1	Pickup IL3+C/Arranque 50BF_L3	Pickup IL3+C/Arranque 50BF_L3	Post-Falla 3
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	300,0 ms	200,0 ms
DISP. L1_52J14	0	0	0	0	0	0
DISP. L2_52J14	0	0	0	0	0	0
DISP.L3_52J14	0	0	0	1	0	0
ENVIO DDT	0	0	0	0	1	0
DISP. 50BF_ET2/0	0	0	0	0	1	0
DSIP.L1_52J14 BOB2	0	0	0	0	0	0
DSIP.L2_52J14 BOB2	0	0	0	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed



10.4 Operacion 50BF_Fase L123:

Test Settings

State	Prefalla	Pickup IL123+S/ Arranque 50BF_L123	Post Falla 1	Pickup IL2+C/Arranque 50BF_L123	Pickup IL123+C/ Arranque 50BF_L123	Post-Falla 2
I L1	800,0 mA 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	800,0 mA -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	800,0 mA 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 11:54:11	Test End:	04-abr.-2019 11:54:19
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Retrip 50BF (T1)	Pickup IL2+C/Arranque 50BF_L123	Pickup IL2+C/Arranque 50BF_L123	DISP. L1_52J140>1	50,00 ms	30,00 ms	30,00 ms	76,70 ms	26,70 ms	+
Disp. 50BF_Etapa 2	Pickup IL2+C/Arranque 50BF_L123	Pickup IL2+C/Arranque 50BF_L123	DISP. 50BF_ET2/0 0>1	200,0 ms	30,00 ms	30,00 ms	226,1 ms	26,10 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

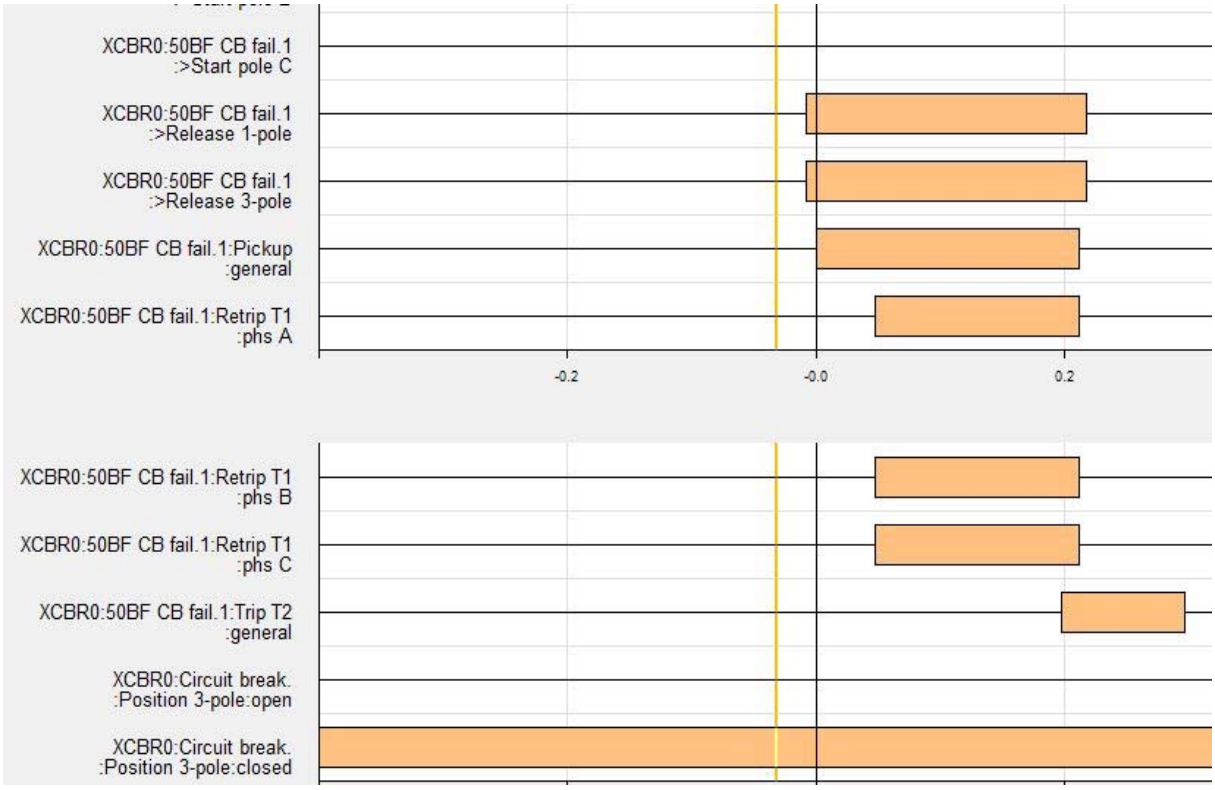
	Prefalla	Pickup IL123+S/ Arranque 50BF_L123	Post Falla 1	Pickup IL2+C/Arranque 50BF_L123	Pickup IL123+C/ Arranque 50BF_L123	Post-Falla 2
Assess	+	+	+	+	+	+
Tolerance	0,000 s	0,000 s	0,000 s	300,0 ms	300,0 ms	200,0 ms

DISP. L1_52J14	0	0	0	1	0	0
DISP. L2_52J14	0	0	0	1	0	0
DISP.L3_52J14	0	0	0	1	0	0
ENVIO DDT	0	0	0	0	1	0
DISP. 50BF_ET2/0	0	0	0	0	1	0
DSIP.L1_52J14 BOB2	0	0	0	1	0	0
DSIP.L2_52J14 BOB2	0	0	0	1	0	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed



Group end:10. Operacion 50BF_K2 (T1 and T2)

Group:11. Operacion End Fault_50BF E0

Hardware

Test Equipment

Type	Serial Number
CMC356	HE295P

Hardware Check

Performed At	Result	Details
04-04-2019 12:03:24	Passed	

Group:11.1 Verificacion Pickup

11.1.1 Pickup Fase L1 End Fault:

Test Settings

General

No. of ramp states: 1
Total steps per test: 101
Total time per test: 10,100 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	800,0 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	800,0 mA
Sig 1 To	1,300 A
Sig 1 Delta	5,000 mA
Sig 1 d/dt	50,00 mA/s
52J13_Open	1
89J13_Open	0
dt per Step	100,0 ms
Ramp Steps	101
Ramp Time	10,100s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52K2	X
Disp.L2_52K2	X
Disp.L3_52K2	X
Disp. 50BF_ET2/0	1
ENVIO DDT	1
Disp.L1_52K2 BOB2	X
Disp.L2_52K2 BOB2	X
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 04-abr.-2019 12:08:18
Test End: 04-abr.-2019 12:08:29
User Name:
Manager:
Company:

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L1	Ramp 1	ENVIO DDT 0->1 and Disp. 50BF_ET2/0 0->1	I L1	1,200 A	1,205 A	300,0 mA	300,0 mA	5,000 mA	+	60,60 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

11.1.2 Pickup S/C Fase L1 End Fault:

Test Settings

General

No. of ramp states: 1
Total steps per test: 101
Total time per test: 10,100 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	800,0 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	800,0 mA
Sig 1 To	1,300 A
Sig 1 Delta	5,000 mA
Sig 1 d/dt	50,00 mA/s
52J13_Open	0
89J13_Open	0
dt per Step	100,0 ms
Ramp Steps	101
Ramp Time	10,100s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52K2	X
Disp.L2_52K2	X
Disp.L3_52K2	X
Disp. 50BF_ET2/0	1
ENVIO DDT	1
Disp.L1_52K2 BOB2	X
Disp.L2_52K2 BOB2	X
Step back	Yes

Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	04-abr.-2019 12:11:24	Test End:	04-abr.-2019 12:11:36
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

11.1.3 Pickup Fase L2 End Fault:

Test Settings

General

No. of ramp states:	1
Total steps per test:	101
Total time per test:	30,300 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L2 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	800,0 mA -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From **Sig 1 To** **Sig 1 Delta** **Sig 1 d/dt**	800,0 mA 1,300 A 5,000 mA 16,67 mA/s
52J13_Open **89J13_Open**	1 0
dt per Step **Ramp Steps** **Ramp Time**	300,0 ms 101 30,300s
Trigger	Bin
Trigger Logic **Disp.L1_52K2** **Disp.L2_52K2** **Disp.L3_52K2** **Disp. 50BF_ET2/0**	AND X X X 1

ENVIO DDT	1
Disp.L1_52K2 BOB2	X
Disp.L2_52K2 BOB2	X
Step back	No
Delay Time	0,000 s

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 04-abr.-2019 12:14:37
Test End: 04-abr.-2019 12:15:04
User Name:
Manager:
Company:

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L2	Ramp 1	ENVIO DDT 0->1 and Disp.L1_52 K2 BOB2 0->1	I L2	1,200 A	1,205 A	300,0 mA	300,0 mA	5,000 mA	+	74,50 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

11.1.3 Pickup Fase L3 End Fault:

Test Settings

General

No. of ramp states: 1
Total steps per test: 101
Total time per test: 30,300 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz
I L3	800,0 mA 120,00 ° 50,000 Hz
Force abs. Phases	No
Sig 1 From	800,0 mA
Sig 1 To	1,300 A
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J13_Open	1
89J13_Open	0
dt per Step	300,0 ms

Ramp Steps	101
Ramp Time	30,300s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52K2	X
Disp.L2_52K2	X
Disp.L3_52K2	X
Disp. 50BF_ET2/0	1
ENVIO DDT	1
Disp.L1_52K2 BOB2	X
Disp.L2_52K2 BOB2	X
Step back	Yes
Delay Time	50,00 ms

Test Module

Name: OMICRON Ramping
Version: 4.00
Test Start: 04-abr.-2019 12:19:33
Test End: 04-abr.-2019 12:20:01
User Name:
Manager:
Company:

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L3	Ramp 1	ENVIO DDT 0->1 and Disp. 50BF_ET2/0 0->1	I L3	1,200 A	1,205 A	300,0 mA	300,0 mA	5,000 mA	+	62,80 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

11.1.4 Pickup Fase L123 End Fault:

Test Settings

General

No. of ramp states: 1
Total steps per test: 101
Total time per test: 30,300 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1
I L1	800,0 mA 0,00 ° 50,000 Hz
I L2	800,0 mA -120,00 ° 50,000 Hz
I L3	800,0 mA 120,00 ° 50,000 Hz

Force abs. Phases	No
Sig 1 From	800,0 mA
Sig 1 To	1,300 A
Sig 1 Delta	5,000 mA
Sig 1 d/dt	16,67 mA/s
52J13_Open	1
89J13_Open	0
dt per Step	300,0 ms
Ramp Steps	101
Ramp Time	30,300s
Trigger	Bin
Trigger Logic	AND
Disp.L1_52K2	X
Disp.L2_52K2	X
Disp.L3_52K2	X
Disp. 50BF_ET2/0	1
ENVIO DDT	1
Disp.L1_52K2 BOB2	X
Step back	Yes
Delay Time	50,00 ms

Test Module

Name:	OMICRON Ramping	Version:	4.00
Test Start:	04-abr.-2019 12:18:32	Test End:	04-abr.-2019 12:19:00
User Name:		Manager:	
Company:			

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pickup_Fase L123	Ramp 1	ENVIO DDT 0->1 and Disp.L1_52 K2 BOB2 0->1	I L1; L2; L3	1,180 A	1,205 A	300,0 mA	300,0 mA	25,00 mA	+	63,90 ms

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

Group end:11.1 Verificacion Pickup

Group:11.2 Operacion End Fault

11.2.1 Operacion End Fault_L1:

Test Settings

State	Prefalla	Falla L1+52K2 Open	Post Falla
I L1	800,0 mA 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 12:22:27	Test End:	04-abr.-2019 12:22:31
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L1+52K2 Open	Falla L1+52K2 Open	Disp. 50BF_ET 2/0 0>1	50,00 ms	30,00 ms	30,00 ms	79,10 ms	29,10 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L1+52K2 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	100,0 ms	200,0 ms
Disp.L1_52K2	0	0	0
Disp.L2_52K2	0	0	0
Disp.L3_52K2	0	0	0
Disp. 50BF_ET2/0	0	0	0
ENVIO DDT	0	1	0
Disp.L1_52K2 BOB2	0	1	0
Disp.L2_52K2 BOB2	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:
Test passed

11.2.2 Operacion End Fault_L2:

Test Settings

State	Prefalla	Falla L2+52K2 Open	Post Falla
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	800,0 mA -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 12:23:34	Test End:	04-abr.-2019 12:23:38
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L2+52K2 Open	Falla L2+52K2 Open	Disp. 50BF_ET 2/0 0>1	50,00 ms	30,00 ms	30,00 ms	70,00 ms	20,00 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L2+52K2 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	100,0 ms	200,0 ms
Disp.L1_52K2	0	0	0
Disp.L2_52K2	0	0	0
Disp.L3_52K2	0	0	0
Disp. 50BF_ET2/0	0	1	0
ENVIO DDT	0	1	0
Disp.L1_52K2 BOB2	0	0	0
Disp.L2_52K2 BOB2	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

11.2.3 Operacion End Fault_L3:

Test Settings

State	Prefalla	Falla L3+52K2 Open	Post Falla
I L1	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	800,0 mA 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 12:24:24	Test End:	04-abr.-2019 12:24:28
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L3+52K2 Open	Falla L3+52K2 Open	Disp. 50BF_ET 2/0 0>1	50,00 ms	30,00 ms	30,00 ms	74,10 ms	24,10 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

State Assessment

	Prefalla	Falla L3+52K2 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	100,0 ms	200,0 ms
Disp.L1_52K2	0	0	0
Disp.L2_52K2	0	0	0
Disp.L3_52K2	0	0	0
Disp. 50BF_ET2/0	0	0	0
ENVIO DDT	0	1	0
Disp.L1_52K2 BOB2	0	1	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed

11.2.4 Operacion End Fault_L123:

Test Settings

State	Prefalla	Falla L123+52 K2 Open	Post Falla
I L1	800,0 mA 0,00 ° 50,000 Hz	1,300 A 0,00 ° 50,000 Hz	0,000 A 0,00 ° 50,000 Hz
I L2	800,0 mA -120,00 ° 50,000 Hz	1,300 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	800,0 mA 120,00 ° 50,000 Hz	1,300 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz

Test Module

Name:	OMICRON State Sequencer	Version:	4.00
Test Start:	04-abr.-2019 12:25:09	Test End:	04-abr.-2019 12:25:13
User Name:		Manager:	
Company:			

Test Results

Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Disp. End Faults	Falla L123+52K 2 Open	Falla L123+52K 2 Open	Disp. 50BF_ET 2/0 0>1	50,00 ms	30,00 ms	30,00 ms	72,00 ms	22,00 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

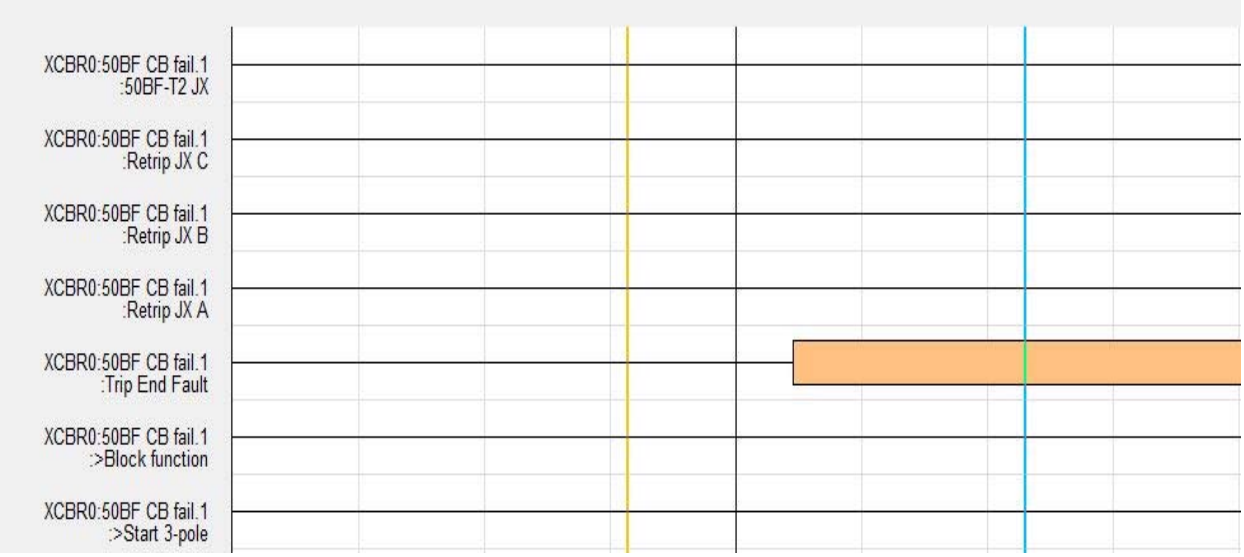
State Assessment

	Prefalla	Falla L123+52 K2 Open	Post Falla
Assess	+	+	+
Tolerance	0,000 s	100,0 ms	200,0 ms
Disp.L1_52K2	0	0	0
Disp.L2_52K2	0	0	0
Disp.L3_52K2	0	0	0
Disp. 50BF_ET2/0	0	1	0
ENVIO DDT	0	1	0
Disp.L1_52K2 BOB2	0	0	0

Assess: + .. Passed x .. Failed o .. Not assessed

Test State:

Test passed



04.04.2019 12:25:12.474 ...		36		Fault log	
04.04.2019 12:25:12.5...	00:00:00:00.063		8	XCBR0:Circuit break.	Position 3-pole
04.04.2019 12:25:12.5...	00:00:00:00.060		7	XCBR0:50BF CB fail.1	Trip End Fault
04.04.2019 12:25:12.5...	00:00:00:00.060		6	Line 1:50/51 OC-3ph-A1:Definite-T 1	Pickup
04.04.2019 12:25:12.5...	00:00:00:00.049		5	XCBR0:50BF CB fail.1	Trip End Fault
04.04.2019 12:25:12.4...	00:00:00:00.010		4	Line 1:50/51 OC-3ph-A1:Definite-T 1	Pickup
04.04.2019 12:25:12.4...	00:00:00:00.000		3	Recording:Fault recorder:Control	Fault number
04.04.2019 12:25:12.4...	00:00:00:00.000		2	Line 1:50/51 OC-3ph-A1:Definite-T 1	Pickup
04.04.2019 12:25:12.4...	-00:00:00:00.010		1	XCBR0:Circuit break.	Position 3-pole
04.04.2019 12:24:27.304 ...		35		Fault log	
04.04.2019 12:24:27.3...	00:00:00:00.062		7	XCBR0:Circuit break.	Position 3-pole
04.04.2019 12:24:27.3...	00:00:00:00.060		6	XCBR0:50BF CB fail.1	Trip End Fault
04.04.2019 12:24:27.3...	00:00:00:00.060		5	Line 1:50/51 OC-3ph-A1:Definite-T 1	Pickup
04.04.2019 12:24:27.3...	00:00:00:00.049		4	XCBR0:50BF CB fail.1	Trip End Fault
04.04.2019 12:24:27.3...	00:00:00:00.000		3	Recording:Fault recorder:Control	Fault number
04.04.2019 12:24:27.3...	00:00:00:00.000		2	Line 1:50/51 OC-3ph-A1:Definite-T 1	Pickup
04.04.2019 12:24:27.2...	-00:00:00:00.010		1	XCBR0:Circuit break.	Position 3-pole
04.04.2019 12:23:37.244 ...		34		Fault log	
04.04.2019 12:23:37.3...	00:00:00:00.062		7	XCBR0:Circuit break.	Position 3-pole
04.04.2019 12:23:37.3...	00:00:00:00.060		6	XCBR0:50BF CB fail.1	Trip End Fault
04.04.2019 12:23:37.3...	00:00:00:00.059		5	Line 1:50/51 OC-3ph-A1:Definite-T 1	Pickup
04.04.2019 12:23:37.2...	00:00:00:00.049		4	XCBR0:50BF CB fail.1	Trip End Fault
04.04.2019 12:23:37.2...	00:00:00:00.000		3	Recording:Fault recorder:Control	Fault number
04.04.2019 12:23:37.2...	-00:00:00:00.001		2	Line 1:50/51 OC-3ph-A1:Definite-T 1	Pickup
04.04.2019 12:23:37.2...	-00:00:00:00.008		1	XCBR0:Circuit break.	Position 3-pole
04.04.2019 12:22:30.483 ...		33		Fault log	
04.04.2019 12:22:30.5...	00:00:00:00.070		7	Line 1:50/51 OC-3ph-A1:Definite-T 1	Pickup
04.04.2019 12:22:30.5...	00:00:00:00.063		6	XCBR0:50BF CB fail.1	Trip End Fault
04.04.2019 12:22:30.5...	00:00:00:00.063		5	XCBR0:Circuit break.	Position 3-pole
04.04.2019 12:22:30.5...	00:00:00:00.050		4	XCBR0:50BF CB fail.1	Trip End Fault
04.04.2019 12:22:30.4...	00:00:00:00.000		3	Recording:Fault recorder:Control	Fault number
04.04.2019 12:22:30.4...	00:00:00:00.000		2	Line 1:50/51 OC-3ph-A1:Definite-T 1	Pickup
04.04.2019 12:22:30.4...	-00:00:00:00.014		1	XCBR0:Circuit break.	Position 3-pole

Group end:11.2 Operacion End Fault

Group end:11. Operacion End Fault_50BF E0